A4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

IMPORTANT INSTRUCTIONS:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2. **PART ONE** is to be answered in the **OMR ANSWER SHEET** only supplied with the question paper as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS **TOTAL MARKS: 100**

(PART ONE – 40; PART TWO – 60)

PART ONE

(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

1.1 A combinational circuit which converts binary information from n coded inputs to maximum of 2^n^ unique output is
A) Multiplexer
B) Decoder
C) Encoder
D) None of the above

1.2 The largest Signed number which can be accommodated in 2 byte register is
A) 2^n^
B) 2^n^ – 1
C) 2^n^
D) None of the above

1.3 If the second part of the instruction code specifies the address of an operand, the instruction is said to have
A) Direct Address
B) Immediate Address
C) Indirect Address
D) D. None of the above

1.4 The which of the following example refers to Reverse Polish Notation?
A) A + B
B) +AB
C) AB+
D) None of the above

1.5 +0 or -0 may appear in arithmetic operation in
A) Signed-1's complement representation
B) Signed-2's complement representation
C) Signed- magnitude representation
D) None of the above

1.6 Electromechanical and electromagnetic devices are termed as
A) Computer
B) Peripherals
C) DMA
D) None of the above

1.7 It is customary to specify the asynchronous data transfer between two independent devices by
A) Means of timing diagram
B) Using common clock pulse rate
C) Using buses for burst transfer
D) None of the above

1.8 For electromechanical devices with moving parts, the access time is
A) The time to position read-write head to a location
B) The time to transfer data to or from the device.
C) The time to position read-write head to location plus the time to transfer data to or from the device.
D) None of the above

1.9 Locality of reference property is exploited in introducing
A) Virtual memory
B) Cache
C) RAM
D) None of the above

1.10
```
MOV  CX, 0
        MOV  AX,1
ONE:
        INC AX
        LOOP ONE
```
In the above assembly program segment, how many times the loop ONE will be executed?
A) One time
B) Many times
C) Zero time
D) None of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

2.1 Multi-input AND gate is sensitive to logic 0 on any one of of its inputs, irrespective of any values at other input.
2.2 JK Flip- Flop produces an indeterminate next state when J = K = 1.
2.3 Addition of largest signed number to any signed number will always generate overflow condition.
2.4 Entire register transfer operation from the source registers through ALU and into the destination register can be performed in two clock pulse period.
2.5 One-address instruction uses an implied accumulator (AC) register for all data manipulation.
2.6 A software interrupt is initiated from signals which occur in the hardware of CPU.
2.7 In serial asynchronous data transfer, the stop bit is always in 0- state and frame the end of character to signify the idle or wait state.
2.8 The ROM does not need a read control line.
2.9 By keeping frequently accessed instruction and data in cache memory, the average memory access time approaches the access time of cache.
2.10 Every assembly statement is converted to machine language statement by assembler.

3. Match words and phrases in column X with the closest related meaning / word(s) / phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

X		Y	
3.1	Representation of input-output relationship of binary variable for each gate	**A.**	Register transfer micro-operation
3.2	A triangle graphic symbol in logic gate	**B.**	trap
3.3	The content remains unchanged in one of the micro-operation.	**C.**	AL
3.4	Instruction containing the operand itself	**D.**	Hit ratio
3.5	Input – Output instruction	**E.**	Truth table
3.6	Another name for internal interrupt	**F.**	Booth Algorithm
3.7	A multiplication algorithm	**G.**	Buffer
3.8	To turn power on and starting execution of initial program	**H.**	Immediate instruction
3.9	Performance of Cache memory	**I.**	INP
3.10	Moving 126Fh to AX, results in 6Fh in which register of Assembly statement	**J.**	Computer start up
		K.	Arithmetic Micro-operation
		L.	Access time
		M.	Direct Instruction

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

A.	Four	**B.**	Access time	**C.**	Normalized
D.	Associative	**E.**	IR	**F.**	Asynchronous
G.	Mapping	**H.**	Serial	**I.**	NOR
J.	Software interrupt	**K.**	Synchronous	**L.**	In IEEE format
M.	Parallel				

4.1 ________ gate is the complement of OR gate.

4.2 A floating – point number is said to be ________ if the most significant digit of the mantissa is non-zero.

4.3 ________ contains the instruction which is being executed.

4.4 ________ is a special call instruction which behaves like interrupt rather than a subroutine call.

4.5 External interrupt is ________ with the program.

4.6 ________ transmissions can be synchronous or asynchronous.

4.7 Average time required to reach a storage location in memory and obtain its content is called ________.

4.8 ________ memory stores both address and content of memory word.

4.9 Transformation of data from main memory to cache memory is referred to as ________ process.

4.10 There are ________ segments registers in 8086 assembly language.

PART TWO

(Attempt any **FOUR** questions)

5.

a) Show that a JK – flip – flop can be converted to D flip – flop with an invertor between J and K inputs.

b) What is half adder? Draw its logic diagram using OR gate and AND gate and its truth table. Draw the block diagram to show implementation of universal NOR gate through half adder.

(7+8)

6.

a) i) Add (1AFE) + (5F11) =

ii) Write the sum of (i) in binary and give its 2's complement also.

b) Explain the following addressing modes with help of suitable examples:

i) Indexed Addressing Mode

ii) Register Addressing Mode

iii) Indirect Addressing Mode

iv) Immediate Addressing Mode

(7+8)

7.

a) Write an assembly language program segment to find the number of times the letter 'Z' has appeared in the given string of 50 characters at 'MSG'. Put the result at NUMZ which is defined as word.

b) How does a program execute in the computer?. Enumerate the phases of 'Instruction Cycle'. Draw the flow chart of Instruction Cycle and explain any one phase in detail.

(7+8)

8.

a) Show the step-by-step multiplication process using Booth's Algorithm for (+15) x (-13). Assume 5-bit registers that hold signed numbers. The multiplicand is +15.

b) Differentiate between synchronous and asynchronous serial transmission. Also, explain in detail the serial asynchronous data transmission technique used in interactive terminals. What will be bit time and baud rate, if transfer rate of terminal is 10 characters per second?

(8+7)

9.

a) What is DMA? How is CPU placed in idle state? Explain DMA transfer through block diagram.

b) The access time of a cache memory is 100 ns. and that of main memory 1000ns. It is estimated that 80 percent of memory request are for read and remaining 20 percent for write. The hit ratio for read accesses only 0.9. A write – through procedure is used.

i) What is average access time of the system considering only memory read cycles?

ii) What is average access time of the system for both read and write cycles?

iii) What is hit ratio taking into consideration the write cycle?

(8+7)