Annexure – I
Course Curriculum

1: *Advanced Digital Design*

Duration: 35 Hours

Objective

The objective of the course is to provide understanding of the entire logic design process with the analysis from combinational and sequential digital circuit design.

Course Description

- Combinational Circuit Design
- Sequential Circuit Design
- Design of controller and Data path units
- State Machines
- Controller Design using FSMs & ASMs
- Design Examples & Case Studies

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Analyse combinational and sequential circuit design concepts.
- Develop FSMs & ASMs for the given problems.

Text Books:

1. Modern Digital Electronics. Author, R P Jain. Edition, 3. Publisher, Tata McGraw-Hill Education
2. Wakerly, John F. Digital Design Principles and Practices,

2: VHDL: Language and Coding for Synthesis

Duration: 70 Hours

Objective

The objective of the course is to provide understanding of the techniques essential to the VHDL programming for Verification and Testing.

Course Description

- Language Constructs, Data types

- Design Styles
- Behavioral Modeling, Dataflow Modeling
- Structural Modeling
- Generics and Configurations
- Subprograms and overloading
- Packages and Libraries
- Advanced features of VHDL
- Test Bench Design and Coding
- Synthesis issues
- Mini Project and Case Studies

Learning Outcomes

On completion, the participants will be able to:

- Write Verilog code, compile, simulate and execute on any VLSI design platform.
- Perform verification and testing

Reading List

1. VHDL Programming By Example By Douglas Perry-PHI

3: Verilog HDL: Language and Coding for Synthesis

Duration: 105 Hours

Objective

The objective of the course is to provide understanding of the techniques essential to the Verilog programming for Verification and Testing.

Course Description

- Introduction to Verilog HDL & Hierarchical Modeling Concepts
- Lexical Conventions & Data Types
- System Tasks & Compiler Directives
- Modules, Ports and Module Instantiation Methods
- Gate Level Modeling
- Dataflow Modeling
- Behavioral Modeling
- RTL Design and Logic Synthesis and Synthesis issues
- Design Verification using Test benches
- Mini-project and Case Studies

Learning Outcomes

After successful completion of the module, the students shall be able to:

- Write Verilog code, compile, simulate and execute on any VLSI design platform.
- Perform verification and testing

Reading List

1.Verilog HDL, 2/E By Samir Palnitkar,Pearson Education

4: RTL Verification (System Verilog, UVM)

Duration: 175 Hours

Objective

SystemVerilog is an IEEE approved Hardware Description Language. It provides superior capabilities for system architecture, design, and verification. SystemVerilog enables to rapidly develop RTL code, easily maintain code, and minimize the occurrence of situations where the RTL code simulates differently than the synthesized netlist.

Course Description

Functional Verification – Concepts, Simulators, Coverage and Metrics, Introduction to Verification Methodologies ,Testing strategy – Directed and random Testing, Test Cases Vs Test Benches, Verification Components (Drivers, Checkers, Monitors, Scoreboards etc),Case study of a Verification IP.

System Verilog, Object oriented programming for ASIC Design & Verification, Functional Verification, Assertion based verification, Coverage Driven Verification, Coverage Analysis, PLI and DPI Basics, Universal Verification Methodology , UVM Components and practices, Verification IP Design.

Learning Outcomes

On completion, the participants will be able to:

- Perform the verification and testing.
- Generate UVM for the Design functions.

Reading List

1. Principles of Verifiable RTL Design by Bening, Lionel, Foster, Harry D.
2. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features by Chris Spear

Qualification File: PG Diploma in VLSI & Embedded Hardware Design (Level 8)

5: FPGA Design Methodology and Prototyping

Duration:70 Hours

Objective

FPGAs are the present day tool for implementing many embedded applications. A basic understanding of digital electronics is very useful for the proper understanding of this topic. Basics of communication are also covered for further applications.

The course is structured to include the learning of Verilog HDL syntax and the architecture of most prominent vendor in the FPGA market, Xilinx FPGAs and Altera FPGAs. Hands own experiments and a mini-project are included in the module.

Course Description

- Introduction to Programmable Logic and FPGAs
- Popular CPLD & FPGA Families
- Architecture of popular Xilinx and Altera FPGAs
- FPGA Design Flow Altera Quartus II
- FPGA Design Flow Xilinx ISE
- Implementation Details
- Advanced FPGA Design tips
- Logic Synthesis for FPGA
- Static Timing Analysis
- Design problems using Xilinx Platforms
- Design problems using Altera Platforms
- Case Studies on FPGA Based implementations
- IP Reuse Methodology
- Soft IP vs Hard IP
- IP Design Process & System Integration with reusable IP

Learning Outcomes

On completion, the participants will be able to:

- Apply Verilog HDL for FPGA Programming
- Implement Digital Circuits on Xilinx FPGAs and Altera FPGAs using Verilog HDL

Reading List

- FPGA Users Guides and Datasheets From Xilinx & Altera

6 CMOS Logic & Physical Design

Duration: 70 Hours

Objective

CMOS is a technology for constructing integrated circuits. CMOS gate designs is a much wider allowable range of power supply voltages. The course is structured to include the learning of CMOS logic design with their characteristic features for designing an IC.

Course Description

MOS Fundamentals, MOS Switches & Designs, Transmission Gates, Inverter – DC, AC Characteristics, Combinational and Sequential Logic, Introduction to Layout Tools
Introduction to IC Layout, IC Layout Design tools, RTL to GDS II, Introduction to Physical Verification (DRC, LVS, SoftCheck, Antenna Effect and DFM), Layout design rules & techniques. Circuit examples.

Learning Outcomes

On completion, the participants will be able to:

- Design all possible logic gates by CMOS technology.
- Gain the knowledge on IC layout Design methodologies.

Reading List

- CMOS VLSI Design: A Circuits and Systems Perspective: United States Edition by Neil Weste ,David Harris
- CMOS Logic Circuit Design Hardcover by John P. Uyemura

7:Embedded Controller Based Product Design

Duration: 105 Hours

Objective

The objective of this module is to help fresh graduates and practicing engineers to enhance their knowledge and skills of embedded product design covering the various aspects of product development process and design of a stand- alone embedded system.

Course Description

- Quality principles and tools
- Product Development Process
- System level design using hardware and software
- Hardware and software integration issues and testing
- Hardware and software co-verification
- Component cost and costing in product design

- Case studies of real life designs
- Industrial Design
- Project Management (PERT/CPM) MS Project
- Interconnection design & EDA tools
- Thermal Design
- Documentation
- Team work and communication
- Embedded Product design Syndicate
- EMI/EMC
- Case study of Microcontroller based Design
- Project Design phase
- Hardware design and construction
- Software design and development
- Integration and debugging of hardware and software
- Final testing
- ORCAD Schematic and PCB Layout
- Mini Project

Learning Outcomes

After successful completion of the module, the students shall be able

a) Apply product development process for realization of the product
b) Design and develop a standalone Embedded System using Microcontrollers through conceptual design, PCB Design, PCB Assembly, Testing, Integration etc.

Reading List

1. Product Design & Development – Karl T Ulrich & Steven D. Eppinger; Mc Graw Hill
2. Relevant Data sheets and application notes

8: Project Work

Duration: 210 Hours

Course Description

The students can select hardware, software or system level projects. The project can be implemented using EDA tools or FPGA boards which students have studied and used during the course. A total product or project can be selected.