QUALIFICATION FILE – Standalone NOS

Fundamentals of VLSI Verification

☐ Horizontal/Generic ☐ Vertical/Specialization

☒ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☒OEM

NCrF/NSQF Level: 5

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

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<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version (Will be issued after NSQC approval.)</td><td>NG-05-EH-02905-2024-V1-NIELIT</td><td>5. NCrF/NSQF Level: 5</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">This Standalone NOS covers the essentials of VLSI verification, focusing on developing comprehensive test benches and utilizing scripting languages for test automation. Students learn the basics of Verilog HDL for verification, including lexical conventions, data types, operators, and modeling techniques (gate level, data flow, and behavioral). The module explores hierarchical modeling, design methodologies, and test benching for effective verification. It introduces verification architecture and flow, design verification using Verilog HDL, and coverage-driven verification. Practical skills in test automation, writing assertions, and developing scripts for test case generation, regression testing, and result analysis are also emphasized.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
<table>
<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Relevant Experience (with Specialization - if applicable)</th></tr>
<tr><td>1</td><td>2nd year of UG in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches</td><td>NA</td></tr>
<tr><td>2</td><td>3 Years of Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 10th</td><td>1.5 Years</td></tr>
<tr><td>3</td><td>2 Year of diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 12th</td><td>NA</td></tr>
</table></td></tr>
</table>

		4 | NSQF Level 4.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches | 1.5 Years 5 | NSQF Level 4 Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches | 1.5 Years **b. Age**: 18 Years
8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	2 Credits **9. Common Cost Norm Category (I/II/III)** *(wherever applicable)***:** Category-I
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☒**Offline** ☐ **Online** ☐ **Blended** **Training Delivery Mode** | **Theory (Hours)** | **Practical (Hours)** | **Total (Hours)** Classroom (offline) | 30 | 30 | 60 Training shall be conducted in any of the 3 modes depending on the regional need. *(Refer Blended Learning Annexure-V for details)*
12.	**Assessment Criteria**	**Theory (Marks)** | **Practical (Marks)** | **Project (Marks)** | **Viva (Marks)** | **Total (Marks)** | **Passing %age** 100 | 60 | 20 | 20 | 200 | 50 The centralised online assessment is conducted by the Examination Wing, NIELIT Headquarters.

13.	**Is the NOS Amenable to Persons with Disability**	☒ **Yes** ☐ **No If "Yes", specify applicable type of Disability:** **a.** Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims **b.** Visual Impairment: Low Vision	
14.	**Progression Path After Attaining the Qualification, wherever applicable** *(Please show Professional and Academic progression)*	*Design/Application Engineer/Team Lead / Project Manager*	
15.	**How participation of women will be encouraged?**	Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women's participation under other schemes launched by the Government from time to time.	
16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	Qualification files available in English & Hindi Language.	
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	**Name:** Jayaraj U Kidav **Email:** jayaraj@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Ishant Kumar Bajpai **Email:** ishant@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Deepam Dubey **Email:** deepamdubey@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Sreejeesh S.G **Email:** sreejeesh@nielit.gov.in **Website:** https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 Years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLS Design
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI Design
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No *(If "Yes", details to be provided in Annexure)* Available at Annexure-II
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B.Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech
4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted

5.	**Tools and Equipment Required for Assessment**	Same as for training ☒ Yes ☐ No

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided:
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure: Industry Validation**	*Available at* Annexure-III: Industry Validation
4.	**Annexure: Training Details**	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning

6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	● Understanding port types, data types, operators, numbers, vectors, arrays, compiler directives, and system tasks in Verilog HDL. ● Knowledge of logic primitives, gate-level modeling, data flow modeling, and behavioral modeling techniques in Verilog for digital design representation. ● Familiarity with hierarchical modeling, module instantiation rules, test bench development, and verification techniques such as coverage-driven verification, test automation, assertions, and writing test cases using Verilog HDL.	The job role demands specialized theoretical and practical skills for applying Verilog HDL in variable contexts, addressing both routine and non-routine tasks, such as developing test benches, performing verification, and optimizing test cases for digital systems, consistent with Level 5 requirements.	5
Professional and Technical Skills/ Expertise/ Professional Knowledge	● Ability to utilize Verilog HDL for digital design, including knowledge of lexical conventions, data types, operators, vectors, arrays, compiler directives, and system tasks.	The qualification emphasizes comprehensive factual and theoretical knowledge of digital design and verification within broad contexts, aligning with Level 5	5

	● Skills in implementing logic primitives, gate-level modeling, data flow modeling, and behavioral modeling to design and simulate digital circuits effectively.	descriptors where a professional applies advanced techniques for creating efficient and accurate digital systems.	
Employment Readiness & Entrepreneurship **Skills & Mind-set/Professional Skill**	● Ability to understand and apply Verilog HDL lexical conventions, including port types, data types, operators, and system tasks, essential for digital design and verification roles. ● Competence in hierarchical modeling and test benching methodologies, including module instantiation rules and design abstraction techniques. Understanding verification architectures, flow, and types of test benches prepares individuals for verification engineering roles. ● Familiarity with scripting languages for test automation enhances productivity and efficiency in verification tasks, crucial for managing large-scale projects and meeting stringent deadlines in the semiconductor industry.	The job role involves a wide range of cognitive and practical skills to solve specific problems in digital verification engineering, fostering employment readiness and entrepreneurial capabilities through systematic application of scripting, debugging, and coverage-driven methodologies.	5
Broad Learning Outcomes/Core Skill	Gain comprehensive knowledge and skills in Verilog HDL for verification, covering lexical conventions, design abstractions, and modeling techniques, alongside proficiency in verification methodologies including test benches, coverage-driven verification, and test automation using scripting languages, essential for roles in digital design and verification engineering.	The syllabus equips candidates with advanced logical, mathematical, and technical communication skills necessary for structured problem-solving, consistent with Level 5 descriptors focused on organizing, analyzing, and presenting information in defined technical environments.	5

Responsibility	Ability to manage system resources effectively by planning, estimating, coordinating, and controlling the activities involved in the design and development of verification tasks/projects.	Candidates are expected to take full responsibility for the accuracy and efficiency of their outputs and may oversee group activities in design and verification processes, aligning with Level 5 descriptors emphasizing responsibility for tasks and teamwork in technical contexts.	5

Annexure-II: Tools and Equipment (lab set-up)

LIST OF EQUIPMENT (For a batch of 30 students)

	Description	Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB

			Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
2	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
3	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
4	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba, Medinipur	9434996748	bginfotech2007@gmail.com
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com

6	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com
7	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2024-25	500	200	20
2025-26	500	200	20
2026-27	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	☐Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
2	☐Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
3	☐Showing Practical Demonstrations to the learners	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet,	20:80

		MS Teams, etc.	
4	☐Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
5	☐Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
6	☐Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	☐On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Design Software	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. Description:

This NOS is designed to provide a comprehensive understanding of the essential principles, methodologies, and tools involved in the verification of Very Large Scale Integration (VLSI) circuits. This educational program begins by establishing a solid foundation in digital design concepts, ensuring that participants possess a strong grasp of the fundamental building blocks of VLSI systems. The curriculum then progresses to explore the intricacies of verification methodologies, emphasizing the significance of thorough testing and validation in the semiconductor design process.

2. Scope:

The scope covers the following:

- This includes understanding lexical conventions such as port types, data types, operators, and system tasks. It covers design abstractions like logic primitives, gate-level modeling, data flow modeling, and behavioral modeling in Verilog HDL.
- Students will learn hierarchical modeling methodologies and port connection rules. Concepts include module instantiation by port name or order, creating test benches, and managing design abstractions files essential for structured verification.

- The syllabus emphasizes verification architecture and flow, encompassing design verification using Verilog HDL and various types of test benches. It covers coverage-driven verification techniques, writing effective test cases, and employing scripting languages for test automation, preparing students for rigorous verification practices in digital design.

3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

Basics of Verilog HDL for verification

- Understanding of Verilog HDL lexical conventions including port types, data types, operators, numbers, vectors, arrays, compiler directives, and system tasks.
- Ability to implement Verilog HDL design abstractions such as logic primitives, gate-level modeling, data flow modeling, and behavioral modeling.

Hierarchal Modeling and test benching for verification

- Competency in applying design methodologies and adhering to port connection rules in hierarchical modeling.
- Capability to develop and utilize test benches effectively for verifying Verilog HDL designs.

Introduction to Verification, Verification Types, Verification Architecture and Flow

- Understanding of the verification process, including verification architecture and flow in digital design projects.
- Knowledge of various verification types such as test automation, assertions, and coverage-driven verification.

Test Automation and Scripting

- Proficiency in using scripting languages for test automation in Verilog HDL verification.
- Capability to develop scripts to automate test cases, improve verification efficiency, and manage verification components.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Comprehensive understanding of Verilog HDL basics, encompassing lexical conventions, design abstractions, and modeling techniques like gate-level and behavioral modeling.
- Proficiency in hierarchical modeling methodologies, including module instantiation rules and the utilization of test benches for structured design verification.
- Knowledge and application of advanced verification techniques, encompassing verification architecture, test automation scripting, and coverage-driven verification to ensure robust design validation.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1: Ability to write and understand Verilog HDL code, including lexical conventions, design abstractions, and behavioral modeling techniques.

GS2: Capability to apply hierarchical modeling methodologies for structured design, manage port connections, and instantiate modules using different methods.

GS3: Skills in verification architecture, flow management, and employing various verification techniques such as test automation, assertions, and coverage-driven verification.

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project Marks	Viva Marks
Fundamentals of VLSI Verification **NOS Code : NIE/ELE/N0117**	**Basics of Verilog HDL for verification**	25	15	20	5
	• Understanding of Verilog HDL lexical conventions including port types, data types, operators, numbers, vectors, arrays, compiler directives, and system tasks.	-	-		-
	• Ability to implement Verilog HDL design abstractions such as logic primitives, gate-level modeling, data flow modeling, and behavioral modeling.	-	-		-
	Hierarchal Modeling and test benching for verification	25	15		5
	• Competency in applying design methodologies and adhering to port connection rules in hierarchical modeling.	-	-		-
	• Capability to develop and utilize test benches effectively for verifying Verilog HDL designs.	-	-		-
	Introduction to Verification, Verification Types, Verification Architecture and Flow	25	15		5
	• Understanding of the verification process, including verification architecture and flow in digital design projects.	-	-		-
	• Knowledge of various verification types such as test automation, assertions, and coverage-driven verification.	-	-		-
	Test Automation and Scripting	25	15		5
	• Proficiency in using scripting languages for test automation in Verilog HDL verification.	-	-		-
	• Capability to develop scripts to automate test cases, improve verification efficiency, and manage verification components.	-	-		-
Total Marks -200		**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.