भारतीय प्रौद्योगिकी संस्थान गुवाहाटी
INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI

QUALIFICATION FILE

RTL and FPGA based System Designer

☒ Short Term Training (STT) ☐ Long Term Training (LTT) ☐ Apprenticeship

☐ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☐ OEM

NCrF/NSQF Level: 5.5

Submitted By:

IIT Guwahati,

Amingaon, North Guwahati,

Guwahati,

Assam 781039

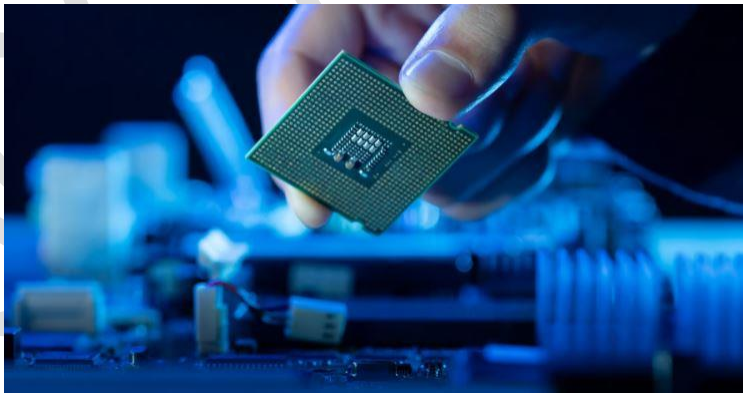

Table of Contents

Section 1: Basic Details

1.	**Qualification Name**	**RTL and FPGA based System Designer**	
2.	**Sector/s**	**Electronics and Electrical**	
3.	**Type of Qualification: ☒ New ☐ Revised ☐ Has Electives/Options ☐OEM**	**NQR Code & version of existing/previous qualification: NA** *(change to previous, once approved)*	**Qualification Name of existing/previous version: NA**
4.	**a. OEM Name** **b. Qualification Name** (*Wherever applicable)*		
5.	**National Qualification Register (NQR) Code & Version** (*Will be issued after NSQC approval)*	QG-5.5-EH-04147-2025-V1-IITG	**6. NCrF/NSQF Level: 5.5**
7.	**Award (Certificate/Diploma/Advance Diploma/ Any Other** *(Wherever applicable specify multiple entry/exits also & provide details in annexure)*	Certificate	
8.	**Brief Description of the Qualification**	This course is aimed at providing the front-end knowledge of VLSI systems design including FPGA implementation of learner's design. RTL design and FPGAs can contribute to environmental sustainability in various ways, primarily through their impact on power efficiency, resource utilization, and flexibility.	
9.	**Eligibility Criteria for Entry for Student/Trainee/Learner/Employee**	**a. Entry Qualification & Relevant Experience:**	

S. No.	Academic/Skill Qualification (with Specialization - if applicable)	Required Experience (with Specialization - if applicable)
1	Completed 4-year UG in Engineering **	No experience required
2	Completed 2 Years Diploma in relevant field after class 12 **	1.5 Year of Relevant Experience *

		3 | NSQF level 5 Previous relevant qualifications | 1.5 Years relevant experience * ** Experience in IT, Electronics, Electrical, Computer Science field *Knowledge of programming **b. Age:**
10.	**Credits Assigned to this Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	20 — **11. Common Cost Norm Category (I/II/III)** *(wherever applicable)***: NA**
12.	**Any Licensing requirements for Undertaking Training on This Qualification** *(wherever applicable)*	(open source platform/software) or Free version for Academic purpose
13.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☐**Offline** ☐**Online** ☒**Blended**

Training Delivery Modes	Theory (Hours)	Practical (Hours)	OJT Mandatory (Hours)	OJT Recommended (Hours)	Total (Hours)
Classroom (offline)	45	85	90		600
Online	200	180			

(This qualification can be implemented in online, offline as well as blended mode. In case of Blended mode {Theory 200hrs online 45 hrs. offline}, {Practical 180 hrs. online 85 hrs. offline} {OJT 90 hrs. offline for all modes of delivery})*

1) *Scenario-based open book test & one-to-one online viva.*
2) *Monthly feedbacks will be taken to evaluate if the learners are meeting the intended learning outcomes.*
3) *MCQ (Online) Weekly*
4) *Industry use case Scenarios will be provided as Problem Statements in the LMS Platform for which the projects needs to be deployed, Assessment will be done with the projects Tested and Submitted for evaluation and Practical Hands On for Industry aligned Project Scenarios.*

		5) *In Offline and Blended modes, final assessment will be offline in Test centers across India.* ➢ *Theory Exam 130 Marks* ➢ *Practical Exam 290 Marks (Weekly Coding Assignments (190 Marks) and Final Practical Exam (100 Marks))* ➢ *Project 200 Marks* ➢ *Viva 30 Marks*
14.	**Aligned to NCO/ISCO Code/s** *(if no code is available mention the same)*	2512.0401
15.	**Progression path after attaining the qualification** *(Please show Professional and Academic progression)*	**Entry-Level Roles** 1) RTL Design Engineer: Work on implementing digital logic in RTL, using HDLs like Verilog/VHDL. Focus on design, verification, and optimization of digital circuits. 2) FPGA Engineer: Implement digital designs on FPGA, focusing on real-world constraints like speed, area, and power. Carry out simulation, synthesis, timing analysis, and verification of designs. **Mid-Level Roles (3–5 Years' Experience)** 1) Senior RTL Design Engineer: Lead projects related to RTL design and verification. Optimize RTL code for synthesis, area, and power consumption. 2) Senior FPGA Engineer: Work on system-on-chip (SoC) FPGA architectures, using soft-core processors. Focus on advanced timing closure techniques and high-performance FPGA designs. **Senior-Level Roles (5–10+ Years' Experience)** 1) Principal Engineer/Lead RTL Designer: Lead entire product development cycles, from specification through design, verification, and FPGA implementation. Engage in technical leadership and project management, guiding teams in the development of complex digital systems. 2) FPGA Systems Architect: Work on innovative designs in advanced fields like AI/ML acceleration, autonomous systems, high-performance computing (HPC), etc. Evaluate and select FPGA platforms for system designs.

		3) ASIC/FPGA Design Manager: Manage a team of RTL and FPGA engineers. Work closely with product management, software, and hardware teams to ensure design goals are met.
16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	NA
17.	**Is similar Qualification(s) available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No URLs of similar Qualifications:**
18.	**Is the Job Role Amenable to Persons with Disability**	☒ **Yes** ☒ **No** **If "Yes", specify applicable type of Disability:** Disability in Legs resulting limited mobility
19.	**How Participation of Women will be Encouraged**	Reserved 30% seats for Women
20.	**Are Greening/ Environment Sustainability Aspects Covered** *(Specify the NOS/Module which covers it)*	☒ **Yes** ☐ **No** RTL (Register-Transfer Level) design and FPGA (Field-Programmable Gate Array) technology can contribute to the environment in several ways: 1. Energy Efficiency: RTL design allows for the optimization of digital circuits at a low level. Designers can implement power-efficient architectures and optimize clock gating techniques, reducing overall power consumption. FPGAs, being reconfigurable, enable dynamic power management, allowing specific sections of the chip to be turned off when not in use. (Covered in VLSI Digital Integrated Circuits (NOS Code IITG/VLSI05/NoS/001), VLSI System Design (NOS Code IITG/VLSI05/NoS/002), VLSI DSP (NOS Code IITG/VLSI05/NoS/003) and Hardware description Language (NOS Code IITG/VLSI05/NoS/004) 2. Reduced Hardware Waste: FPGAs are programmable devices, allowing for hardware reuse and reconfiguration. Instead of discarding entire chips when a design changes, FPGAs can be reprogrammed, reducing electronic waste. (Covered in VLSI Digital Integrated Circuits (NOS Code IITG/VLSI05/NoS/001), VLSI System Design (NOS Code IITG/VLSI05/NoS/002), VLSI DSP (NOS Code IITG/VLSI05/NoS/003) and Hardware description Language (NOS Code IITG/VLSI05/NoS/004) 3. Reduced Time-to-Market and Iteration: FPGA technology facilitates rapid prototyping and iteration. Designers can quickly implement and test their designs on FPGAs, reducing the time required to bring a product to market. This can result in fewer physical prototypes and iterations, saving resources and reducing the environmental impact of product development. (Covered in VLSI System Design (NOS Code IITG/VLSI05/NoS/002), VLSI DSP (NOS Code IITG/VLSI05/NoS/003) 4. Space Efficiency: FPGAs can be more space-efficient compared to traditional ASICs (Application-Specific Integrated Circuits) because they can be reprogrammed for different functions. This flexibility allows for the consolidation of multiple functions onto a single FPGA,

		reducing the overall footprint of electronic systems. (Covered in VLSI System Design (NOS Code IITG/VLSI05/NoS/002), VLSI DSP (NOS Code IITG/VLSI05/NoS/003) 5. Energy-Aware Design Practices: RTL design practices include optimizing for performance and power. Designers can employ techniques such as clock gating, low-power state design, and efficient data path implementation to minimize energy consumption. These practices align with environmental sustainability goals. (Covered in VLSI System Design (NOS Code IITG/VLSI05/NoS/002), VLSI DSP (NOS Code IITG/VLSI05/NoS/003) 6. Remote System Updates: FPGAs enable remote updates to the hardware, reducing the need for physical replacements. This is especially relevant in the context of IoT (Internet of Things) devices and infrastructure, where remote updates can extend the lifespan of hardware and reduce the need for frequent replacements. (Covered in VLSI DSP (NOS Code IITG/VLSI06/NoS/003) 7. Customization for Specific Applications: FPGAs can be customized for specific applications, optimizing resource usage for the task at hand. This customization can lead to more efficient and specialized solutions, reducing overall resource consumption. (Covered in Hardware description Language NOS Code (IITG/VLSI05/NoS/004), High Level Synthesis (NOS Code IITG/VLSI06/NoS/002) and FPGA Implementation (NOS Code IITG/VLSI06/NoS/003) In summary, the combination of RTL design practices and FPGA technology can contribute to a more sustainable and environmentally friendly approach in digital design and electronic systems by promoting energy efficiency, reducing waste, and enabling flexible and efficient hardware implementations.	
21.	**Is Qualification Suitable to be Offered in Schools/Colleges**	**Schools ☐ Yes ☒ No Colleges ☒ Yes ☐ No**	
22.	**Name and Contact Details of Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	**Name:** Prof. Gaurav Trivedi **Email:** trivedi@iitg.ac.in **Contact No.:** +91 -8011000783 **Website:** https://www.iitg.ac.in/trivedi/index.html	
23.	**Final Approval Date by NSQC:** *08.05.2025*	**24. Validity Duration: 3 years**	**25. Next Review Date: 08.05.2028**

Section 2: Module Summary

NOS/s of Qualifications
(In exceptional cases these could be described as components)

Mandatory NOS/s:

Specify the training duration and assessment criteria at NOS/ Module level. For further details refer curriculum document.

***Th.**-Theory **Pr.**-Practical **OJT**-On the Job **Man.**-Mandatory Training **Rec.**-Recommended **Proj.**-Project*

S. No	NOS/Module Name	NOS/Module Code & Version *(if applicable)*	Core/ Non-Core	NCrF/NSQF Level	Credits as per NCrF	Training Duration (Hours)					Assessment Marks					
						Th.	Pr.	OJT-Man.	OJT-Rec.	Total	Th.	Pr.	Proj.	Viva	Total	Weightage (%) *(if applicable)*
1.	VLSI Digital Integrated Circuits	IITG/VLSI05/NoS/001	Core	5	2	35	25	0	0	60	30	65	0	5	100	
2.	VLSI System Design	IITG/VLSI05/NoS/002	Core	5	2	25	35	0	0	60	20	60	15	5	100	
3.	VLSI DSP	IITG/VLSI05/NoS/003	Core	5	2	30	30	0	0	60	20	55	20	5	100	
4.	Hardware description Language	IITG/VLSI05/NoS/004	Core	5	5	35	85	30	0	150	20	35	40	5	100	
5.	High Level Synthesis	IITG/VLSI06/NoS/002	Core	5.5	3	25	35	30	0	90	20	40	35	5	100	
6.	FPGA Implementation	IITG/VLSI06/NoS/003	Core	5.5	4	35	55	30	0	120	20	35	40	5	100	
7.	Employability Skills	DGT/VSQ/N0102	Non-Core	5.5	2	60				60			50		50	
Duration (in Hours) / Total Marks					20	245	265	90	0	600	130	290	200	30	650	

Elective NOS/s:

S. No	NOS/Module Name	NOS/Module Code & Version *(if applicable)*	Core/ Non-Core	NCrF/NSQF Level	Credits as per NCrF	Training Duration (Hours)					Assessment Marks					
						Th.	Pr.	OJT-Man.	OJT-Rec.	Total	Th.	Pr.	Proj.	Viva	Total	Weightage (%) *(if applicable)*
1.																
2.																
Duration (in Hours) / Total Marks																

Optional NOS/s:

S. No	NOS/Module Name	NOS/Module Code & Version *(if applicable)*	Core/ Non-Core	NCrF/NSQF Level	Credits as per NCrF	Training Duration (Hours)					Assessment Marks					
						Th.	Pr.	OJT-Man.	OJT-Rec.	Total	Th.	Pr.	Proj.	Viva	Total	Weightage (%) *(if applicable)*
1.																
2.																
Duration (in Hours) / Total Marks																

Assessment - Minimum Qualifying Percentage

*Please specify **any one** of the following:*

Minimum Pass Percentage – Aggregate at qualification level: __70__ % *(Every Trainee should score specified minimum aggregate passing percentage at qualification level to successfully clear the assessment.)*

Minimum Pass Percentage – NOS/Module-wise: ____% *(Every Trainee should score specified minimum passing percentage in each mandatory and selected elective NOS/Module to successfully clear the assessment.)*

Section 3: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	Minimum Masters (Electrical, Electronics or VLSI) with 3 years of experience in RTL Design & Architecture.
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	Minimum Masters (Electrical, Electronics or VLSI) with 5 years of experience in RTL Design & Architecture.
3.	**Tools and Equipment Required for Training**	☒Yes ☐No (*If "Yes", details to be provided in Annexure)*
4.	**In Case of Revised Qualification, Details of Any Upskilling Required for Trainer**	NA

Section 4: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	Minimum Masters (Electrical, Electronics or VLSI) with 3 years of experience in RTL Design & Architecture.
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	Minimum Masters (Electrical, Electronics or VLSI) with 3 years of experience in RTL Design & Architecture.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	Minimum Masters (Electrical, Electronics or VLSI) with 5 years of experience in RTL Design & Architecture.
4.	**Assessment Mode** *(Specify the assessment mode)*	**Online, Offline**
5.	**Tools and Equipment Required for Assessment**	☒ Same as for training ☐ Yes ☐ No *(details to be provided in Annexure-if it is different for Assessment)*

Section 5: Evidence of the need for the Qualification

Provide Annexure/Supporting documents name.

1.	**Latest Skill Gap Study (not older than 2 years) (Yes/No):** Yes
2.	**Latest Market Research Reports or any other source (not older than 2 years) (Yes/No):** Yes
3.	**Government /Industry initiatives/ requirement (Yes/No):** Yes
4.	**Number of Industry validation provided:** 6
5.	**Estimated nos. of persons to be trained and employed:** initial estimate 300 (1st year)
6.	**Evidence of Concurrence/Consultation with Line Ministry/State Departments:** If "No", why:

Section 6: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF level/NSQF descriptors *(Mandatory)*	Provided
2.	**Annexure:** List of tools and equipment relevant for qualification *(Mandatory, except in case of online course)*	**Provided**
3.	**Annexure:** Detailed Assessment Criteria *(Mandatory)*	**Provided**
4.	**Annexure:** Assessment Strategy *(Mandatory)*	**Provided**
5.	**Annexure:** Blended Learning *(Mandatory, in case selected Mode of delivery is "Blended Learning")*	Provided
6.	**Annexure:** Multiple Entry-Exit Details *(Mandatory, in case qualification has multiple Entry-Exit)*	Provided
7.	**Annexure:** Acronym and Glossary *(Optional)*	
8.	**Supporting Document:** Model Curriculum *(Mandatory – Public view)*	Given Separately
9.	**Supporting Document:** Career Progression *(Mandatory - Public view)*	Professional: Member Team Staff (RTL Design and FPGA Implementation) →Senior Member Team Staff Team Staff (RTL Design and FPGA Implementation) → Lead Staff (RTL Design and FPGA Implementation) → Project Manager (RTL Design and FPGA Implementation) Academic: Advance courses in Full chip architecture and data verification.
10.	**Supporting Document:** Occupational Map *(Mandatory)*	VLSI System design, RTL Designer, Product Development.
11.	**Supporting Document:** Assessment SOP *(Mandatory)*	Provided
12.	**Any other document you wish to submit:**	

Annexure: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	• Theoretical and practical knowledge in implementation of RTL code to FPGA boards and verifying their functionality on hardware.	• Possesses advanced knowledge including processes, methods, and techniques about Digital system design and implementation. • Should have a critical understanding of the emerging developments relating digital design strategies? • Understands technological advancements and usage and applies RTL Design. • Undertakes self-study for advancement in skills; demonstrates intellectual independence and good communication. • Acquired advanced knowledge and skills on a wide range of sources for identifying problems and issues relating to the chosen fields of learning, and future improvements	5.5
Professional and Technical Skills/ Expertise/ Professional Knowledge	A Professional must be able to write code of any design/concept to Verilog/HLS and should be able to confirm that code is working file by verifying it on FGPA hardware.	• Possesses a range of advanced cognitive, professional and technical skills required for performing and accomplishing complex tasks relating to the chosen fields of technology/ skills/ job role. • Wide range of cognitive and practical skills required to create innovative and feasible solutions to complex problems and situations in uncertain environment. • Project Management Skills • Understanding and application of techno-Commercial aspect of technology/associated skills or job role. • Skills to adapt to the future of work and to the demands of the fast pace of innovations and technological developments. Social Intelligence	5.5

Employment Readiness & Entrepreneurship **Skills & Mind-set/Professional Skill**	Reasonably good in: ● Verilog coding ● Should be able handle HLS to realize the concepts in High level language and the can be converted into Verilog. ● Should be able handle the FPGA boards and various design implementation on it. ●	• Excellent leadership, Communication, collaboration and organizational skills • Possesses Administrative outlook and leadership traits for managing technical workforce. • Effective mentoring, people management, listening, delegation skills • Organization and Time Management • Creative thinking and Innovation • Good logical and mathematical analysis/ simulation modelling skills • Complete understanding of social, political, natural and work environment. • Organizing, analyzing, interpreting and acting on the information and effectively communicating and presenting/ using its outcome for decision making. • A keen sense of observation, enquiry, and capability for asking relevant/ appropriate questions, • Managing complex technical or professional activities or projects, requiring effective, envisioning, planning & full personal responsibility for output of own work as well as for the outputs of the group as a member of the group/team Apply leadership skills to manage people and resources for achieving organizational objectives and outcomes. Emotional Intelligence	5.5
Broad Learning Outcomes/Core Skill	● Ability to independently develop the logic required for implementing real time embedded systems. ● Ability to understand the social political and natural environment and to organize the information ● Good communication skills to present the embedded real time system-based solutions.	• Applies advance theoretical knowledge and specialized professional and technical skills involving complex variable environment and contexts • Effective understanding, monitoring and supervision of critical parameters and KPIs or others, • Evaluation and improvement of processes, procedures and work or study activities	5.5

	• Concepts/ understanding of Digital system design using Verilog and HLS and its implementation on FPGA hardware.	• Examine and assess the implications and consequences of emerging developments and critical issues. • Make judgement in a range of situations by critically reviewing and consolidating evidences & risks • Constantly and regularly pursue self-paced and self-directed learning to upgrade knowledge and skills that will help accomplish complex tasks or pursue education & research. • Can identifying problems and issues relating to the chosen fields of learning, and ways of future improvements Exercises judgement based on evaluation of evidence from a range of sources to arrive at a solutions to complex real-life problems in chosen fields of technology/ skills/ job role.	
Responsibility	• Understand the job role and follow the organizational policy • Embedded Software Engineer • Team Lead (Embedded Software) • Project Manager (Embedded Software & Real-Time Systems) • Follow safety regulations at work place • Work and interact effectively with colleagues and superiors	•At level 6 the candidate is a Senior Manager/ Senior Technical Manager/ Sr. Product Manager or equivalent. •Is responsible for managing a bigger independent unit/ business activity/ project •Responsible for managing activities like planning, resourcing, processes, people, within broad parameters and with complete accountability for determining, achieving and evaluating personal and group outcomes. •The exercise of full personal responsibility and accountability for the initiatives undertaken and the outputs/outcomes of own work as well as of the group as a team member/ leader	5.5

Annexure: Tools and Equipment (Lab Set-Up)

List of Tools and Equipment

Batch Size: 60

S. No.	Tool / Equipment Name		Quantity for specified Batch size
1	FPGA Boards & Peripherals	Artix-7 OR Quartus boards and IO peripherals.	40
2	Vivado HLS Quartus Matlab	Software tools	40

Classroom Aids

The aids required to conduct sessions in the classroom are:

1. White Board
2. Marker
3. Projector
4. Laptop
5. PPT Presentation
6. Internet with Wi-Fi (Min 2 Mbps Dedicated)

Annexure: Industry Validations Summary

Provide the summary information of all the industry validations in table. This is not required for OEM qualifications.

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID	LinkedIn Profile *(if available)*
1.	Chipspirit Technologies Private Limited	Mr. Mohan Kumar Jindal	CEO & Director	Ground Floor, Vaishnavi Tech Park, Bellandur Gate, Sarjapur Main Road, Ambalipura, Bangalore, Karnataka-560103, https://chipspirit.com/	+91-9500093999	mohan.jindal@chipspirit.com	linkedin.com/in/mohanjindal
2.	CoreEL Technologies (I) Pvt Ltd	Arun John Mathias	Manager - Sandeepani	#21, 7th Main, I Block, Koramangala, Bangalore – 560034. Website: www.coreel.com	+91-9844182555	arun.jm@coreel.com	linkedin.com/in/arun-mathias-501445a
3.	Powai Labs	Reapan Tikoo	Chief Executive	PB 17156 Powai Mumbai 400076 India https://www.powailabs.com/index.htm	+91-9820686855	reapan@powailabs.com	linkedin.com/in/reapan-tikoo-0919a32
4.	Precision Innovations Inc.	Tom Spyrou	CEO	Website:precisioninno.com Email:info@precisioninno.com	+1 (408) 0269	tspyrou@precisioninno.com	linkedin.com/in/tomspyrou

5.	Coverify Systems Technology LLP	Puneet Goel	CTO	Coverify Systems Technology LLP Plot #54, Sector 38, Gurgaon 122005 http://www.coverify.com/	+91-9818131898	puneet@coverify.com	linkedin.com/in/coverification
6	Infinera	Atul Laxmikumar Joshi	Principal SW Engineer	401, Level GF, 3, 4 & 6, Prestige Solitaire Building, Brunton Rd, behind Ajantha Hotel, Craig Park Layout, Ashok Nagar, Bengaluru, Karnataka 560025	+91-8939952217	joshi_atul@yahoo.com	linkedin.com/in/atul-joshi-648104

Annexure: Training & Employment Details

Training and Employment Projections:

Year	Total Candidates		Women		People with Disability	
	Estimated Training #	Estimated Employment Opportunities	Estimated Training #	Estimated Employment Opportunities	Estimated Training #	Estimated Employment Opportunities
1	300	200	50	30	NA	
2	400	250	75	45	NA	
3	500	300	100	60	NA	

Data to be provided year-wise for next 3 years

Training, Assessment, Certification, and Placement Data for previous versions of qualifications:

Qualification Version	Year	Total Candidates				Women				People with Disability			
		Trained	Assessed	Certified	Placed	Trained	Assessed	Certified	Placed	Trained	Assessed	Certified	Placed

Applicable for revised qualifications only, data to be provided year-wise for past 3 years.

List Schemes in which the previous version of Qualification was implemented:

1.
2.

Content availability for previous versions of qualifications:

☐ Participant Handbook ☐ Facilitator Guide ☐ Digital Content ☐ Qualification Handbook ☐ Any Other:

Languages in which Content is available:

Annexure: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

Refer NCVET "Guidelines for Blended Learning for Vocational Education, Training & Skilling" available on:
https://ncvet.gov.in/sites/default/files/Guidelines%20for%20Blended%20Learning%20for%20Vocational%20Education,%20Training%20&%20Skilling.pdf

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	☒Theory/ Lectures - Imparting theoretical and conceptual knowledge	Laptop/ Desktop/ White Board	1:2
2	☒Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Laptop/ Desktop/ White Board	1:2
3	☒Showing Practical Demonstrations to the learners	Laptop/ Desktop/ White Board/Tools and equipment's	1:2
4	☒Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Laptop/ Desktop/Tools and Equipment's	1:2
5	☒Tutorials/ Assignments/ Drill/ Practice	Laptop/ Desktop	1:2
6	☒Proctored Monitoring/ Assessment/ Evaluation/ Examinations	Laptop/ Desktop	0:1
7	☒On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Laptop/ Desktop	0:1

Annexure: Detailed Assessment Criteria

Detailed assessment criteria for each NOS/Module are as follows:

NOS/Module Name	Assessment Criteria for Performance Criteria/Learning Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
VLSI Digital Integrated Circuits (IITG/VLSI05/NoS/001)	PC1.: The performance of MOS circuits will be evaluated based on several parameters such as speed, power consumption, etc.	5	10		
	PC2.: FET design understanding will involve a balance between speed, power, capacitance, and thermal management.	5	10		
	PC3.: MOSFET scaling refers to the process of reducing the physical dimensions of MOSFETs to improve performance, reduce power consumption, and increase transistor density in integrated circuits.	5	10		
	PC4.: Dynamic CMOS design is a technique used in digital logic circuits to improve performance by reducing power consumption and increasing speed and is widely used in high-speed, high-density integrated circuits like microprocessors and memories.	5	20		
	PC5.: Understanding the overall circuit structure and its layout before proceeding to a more detailed, exact physical design.	10	15		5
	Total Marks	30	65		5
VLSI System Design (IITG/VLSI05/NoS/002)	PC1.: The design process involves defining the desired states and transitions, selecting appropriate flip-flops, and developing combinational logic to drive the memory elements.	5	15		
	PC2.: Optimizing the design of the datapath through techniques such as pipelining, parallelism, and hazard management, engineers can significantly enhance the performance and efficiency of digital systems.	5	15		
	PC3.: The design of array subsystems focuses on ensuring efficient data access, low power consumption, and high performance.	5	15		

	PC4.: Understanding the different types of shifters and their applications, designers can leverage these components to enhance performance and optimize resource utilization in a wide range of digital circuits and systems.	5	15		
	PC5.: Project.			15	5
	Total Marks	20	60	15	5
VLSI DSP (IITG/VLSI05/NoS/003)	PC1.: Understand to enhance system performance by overlapping instruction execution and executing multiple tasks simultaneously.	10	15		
	PC2.: The techniques will help to optimize performance, area, and resource utilization. Understanding these concepts allows designers to create more efficient digital systems capable of meeting the demands of modern applications.	6	20		
	PC3: Achieving high performance and low power consumption in modern DSP systems.	4	20		
	PC4.: Project 1			10	
	PC5.: Project 2			10	
	Total Marks	20	55	20	5
Hardware Description Language (IITG/VLSI05/NoS/004)	PC1.: Emphasizes the flow of data through the system, allowing designers to specify how data is processed and transformed by different components.	2	5		
	PC2.: Provides a high-level approach to designing and simulating digital systems.	2	5		
	PC3.: Provides a robust framework for designing digital systems by focusing on the architecture and interconnections of components.	3	5		
	PC4.: Understanding and utilizing conditional statements, looping constructs, event control, and sequential control statements, designers can create flexible and efficient digital systems.	3	5		

	PC5.: Allow designers to create concise, efficient, and modular code that can handle a variety of tasks, from simple bitwise operations to complex data processing algorithms.	3	5		
	PC6.: Tasks, functions, and compiler directives are integral components of HDL design, facilitating code organization, reuse, and synthesis control. Understanding their characteristics and applications is essential for efficient hardware design and ensuring that digital systems meet their specifications.	3	5		
	PC7.: Understanding the structure and components of testbenches in VHDL and Verilog, designers can create effective test environments to ensure their digital designs function correctly.	4	5		
	PC8.: Project 1			10	
	PC9.: Project 2			15	
	PC10.: Project 3			15	5
	Total Marks	20	35	40	5
High Level Synthesis (IITG/VLSI06/NoS/002)	PC1.: Understanding these concepts, designers can create optimized digital systems that leverage high-level programming constructs while meeting stringent performance requirements.	4	8		
	PC2.: Designers can optimize resource utilization and performance.	4	7		
	PC3.: Focus on determining the timing of operations based on dependencies and resource constraints.	4	10		
	PC4.: Designers can create efficient, reliable, and scalable digital systems.	4	10		
	PC5.: Enable designers to create high-performance digital systems.	4	10		
	PC6.: Project 1			15	
	PC7.: Project 2			15	5
	Total Marks	20	45	30	5

FPGA Implementation (IITG/VLSI06/NoS/003)	PC1.: Engineers can create robust and efficient digital designs suitable for various applications.	5	10		
	PC2.: Enables robust data transfer in various applications, from simple sensor interfaces to complex network communications. Understanding the characteristics and requirements of each protocol is essential for effective design	5	10		
	PC3.: Allows designers to create more sophisticated, efficient, and robust digital systems.	5	10		
	PC4.: FPGAs are increasingly used for image processing applications due to their ability to perform parallel processing, their configurability, and their high throughput.	5	5		
	PC5.: Project 1			10	
	PC6.: Project 2			15	
	PC7.: Project 3			15	
	Total Marks	20	35	40	5
Employability Skills (DGT/VSQ/N0102)				**50**	
Grand Total		130	295	195	30

Assessment strategy for a RTL and FPGA based System Designer course that covers VLSI Digital Integrated Circuits, VLSI System Design, Hardware Descriptive Language and FPGA Implementation is crucial to ensure that students acquire the necessary knowledge and skills. Here's a comprehensive assessment strategy divided into four components: Theory, Practical, Viva, and Project.

1. ***Theory Assessment (130 Marks):***

Objective*: To evaluate students' theoretical knowledge and understanding of the course content.*

Components: *Final Exam (100 Marks): A comprehensive final written exam covering all course topics. It should include a mix of multiple-choice questions, short-answer questions, and essay questions to assess different levels of knowledge and critical thinking.*

Class Performance / assessment*: MCQ (Online) Weekly and attendance (30 Marks)*

2. Practical Assessment (290 Marks): *Objective: To assess students' ability to apply their knowledge to practical, real-world scenarios.*

Components: *Weekly Coding Assignments (190 Marks): Assign small coding tasks or exercises related to VLSI and FPGA throughout the course. These assignments should progressively increase in complexity.*

Final Practical Exam *(100 Marks)*

3. Viva Assessment (30 Marks):

Objective: *To evaluate students' oral communication skills, deeper understanding of key concepts, and the ability to explain their work.*

Components: *Individual Viva (20 Marks): Conduct individual oral examinations where students discuss their projects, code, and concepts related to VLSI, HDL and FPGA implementation.*

Group Discussion *(10 Marks): Organize group discussions on current topics and trends in VLSI, HDL, FPGA. This will assess students' ability to collaborate and engage in meaningful discussions.*

4.Project Assessment (200 Marks):

Objective: *To assess students' ability to work on a substantial VLSI, HDL and FPGA project from start to finish, including data collection, analysis, and model development.*

Components: *Project Proposal (30 Marks): Students must submit a detailed project proposal outlining their project's objectives, data sources, methodologies, and expected outcomes.*

Project Progress *(60 Marks): Periodic evaluations of students' project progress, including code reviews, data analysis, and intermediate results with three progress seminars having 20 marks each.*

Final Project Presentation *(60 Marks): Each student presents their project, explaining the problem, approach, results, and insights. The presentation should be followed by a Q&A session.*

Project Report *(50 Marks): A comprehensive project report that includes detailed documentation of the project, data analysis, code, results, and conclusions.*

1. *Assessment System Overview:*
    - *Online assessment will be proctored by engaging a third party. The course access of this third party will be with IIT Guwahati and the participants.*
    - *Offline assessment will be invigilator based. Final assessment will be offline in Test centers across India. Participants who will be doing the course in IIT Guwahati campus will be evaluated by course Instructor. For the participants joining through remote centres will be evaluated by sending external experts from IIT Guwahati.*
    - *Remote centres will be NIT's, Govt Colleges and Private colleges which has adequate resources and good internet connectivity.*
    - *Software licences for this program will be provided by IIT Guwahati and also IIT Guwahati will provide a cloud-based utility setup to access these licences remotely (VPN).*
    - *FPGA prototyping engine is a cloud-based utility provided by Siemens for the remote access and validation of the design implemented in RTL.*
    - *Since this is a FPGA based design (simulation based) so this does not require any post silicon validation kind of lab.*
    - *IIT Guwahati will provide Xilinx and Intel Tools (virtual FPGA Platform)*
    - *IIT Guwahati is procuring a FPGA prototyping platform which can handle up to 400 – 500 participants at a time.*
    - *Certified Assessors will be deployed for executing the assessment.*
2. *Testing Environment:*
    - *The assessment will have scenario based open book test and one-to-one online viva.*
    - *Theory and Practical assessments will have to be completed in the specified time as given in Module Summary.*
3. *Assessment Quality Assurance levels/Framework:*
    - *Question bank is created by the Trainers are again verified by the Master Trainer.*

- *Questions are mapped to all the different modules.*
- *The Assessors and Trainers have the required education and relevant experience in their field with ToA certified ToT Certified.*

4. *Types of evidence or evidence-gathering protocol:*
   - *The assessments will be saved in the cloud/drive and can be assessed whenever required.*
5. *Method of verification or validation:*
   - *Monthly Feedbacks on various aspects of the course, including content clarity, instructional effectiveness, user interface, and overall satisfaction and analyze assessment results to evaluate whether learners are meeting the intended learning outcomes.*
6. *Method for assessment documentation, archiving, and access*

The assessments will be saved in the cloud/drive and can be assessed whenever required.

Justification of the nomenclature of the qualification

The qualification "RTL and FPGA based System Designer" is highly relevant to current industry trends for several compelling reasons:

1. Growing Demand for Customization and Flexibility: Industry trends show an increasing demand for customized and flexible solutions to address diverse application requirements. RTL design and FPGA implementation provide a means to create tailored hardware solutions that can be adapted to specific needs.

2. Acceleration of Prototyping and Time-to-Market: The pace of technological advancements and the need for rapid product development align with the strengths of RTL design and FPGA implementation. These approaches facilitate quick prototyping, iteration, and accelerated time-to-market, crucial aspects in today's competitive business environment.

3. Rise of Edge Computing and IoT: With the rise of edge computing and the Internet of Things (IoT), there is a growing need for efficient and adaptable hardware solutions. RTL design and FPGA implementation allow for the creation of optimized, power-efficient, and application-specific hardware, making them well-suited for edge devices.

4. Increasing Complexity of Digital Systems: The complexity of digital systems is continually increasing, and RTL design serves as an abstraction level that allows designers to work at a register-transfer level, striking a balance between high-level design and low-level hardware description. FPGAs, as reconfigurable devices, are instrumental in managing this complexity by offering flexibility in hardware implementation.

5. Energy Efficiency and Green Computing: Industry trends emphasize a growing awareness of energy efficiency and environmentally conscious computing. RTL design enables designers to optimize for performance and power, and FPGA technology allows dynamic power management, contributing to green computing initiatives.

6. Transition to Heterogeneous Computing: The industry is witnessing a shift towards heterogeneous computing architectures, combining specialized processing units for different tasks. RTL design and FPGA implementation provide a foundation for creating such architectures, allowing designers to tailor hardware to the specific requirements of different processing elements.

7. Advancements in AI and Machine Learning: AI and machine learning applications often demand high-performance and specialized hardware. RTL design and FPGA implementation offer a path to create hardware accelerators customized for AI workloads, aligning with the ongoing trends in the integration of AI into various domains.

8. Focus on Hardware Security: Security is a paramount concern in today's digital landscape. RTL design and FPGA implementation enable designers to incorporate security features directly into the hardware, contributing to the development of secure systems, a critical aspect given the increasing number of cyber threats.

In conclusion, the qualification "RTL design and FPGA implementation" is directly aligned with and justified by the prevailing industry trends, meeting the demand for customization, rapid development, energy efficiency, adaptability, and security in the design and implementation of digital systems.

Annexure: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
ISCO	International Standard Classification of Occupations
NCO	National Classification of Occupations
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework
OJT	On the Job Training

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.
Long Term Training	Long-term skilling means any vocational training program undertaken for a year and above. https://ncvet.gov.in/sites/default/files/NCVET.pdf