QUALIFICATION FILE

Junior Chip Designer (A-Level 'Chip Design')

☒ Short Term Training (STT) ☐ Long Term Training (LTT) ☐ Apprenticeship

☐ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS ☒ Future Skills ☐ OEM

NCrF/NSQF Level: 5

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

NIELIT Bhawan,
Plot No. 3, PSP Pocket, Sector-8,
Dwarka, New Delhi-110077

Table of Contents

Section 1: Basic Details

1.	**Qualification Name**	**Junior Chip Designer (A-Level 'Chip Design')**	
2.	**Sector/s**	**Electronics**	
3.	**Type of Qualification: ☒ New ☐ Revised ☐ Has Electives/Options ☐OEM**	**NQR Code & version of existing/previous qualification: NA**	**Qualification Name of existing/previous version: NA**
4.	**a. OEM Name** **b. Qualification Name** (*Wherever applicable)*	**-**	
5.	**National Qualification Register (NQR) Code &Version** (*Will be issued after NSQC approval)*	QG-05-EH-02594-2024-V1-NIELIT	**6. NCrF/NSQF Level:** 5
7.	**Award (Certificate/Diploma/Advanced Diploma/ Any Other** *(Wherever applicable specify multiple entry/exits also & provide details in annexure)*	Certificate	
8.	**Brief Description of the Qualification**	**Nature:** ❖ This VLSI SoC Design and Verification course equips students with essential industry skills for working on SoC projects. The program covers Verilog HDL coding, FPGA architecture, System Verilog-based verification, and FPGA emulation. Emphasis is on processor architectures, bus protocols, and complex scenario verification. Students learn to design and verify SoCs, crucial for employment readiness. Overall, it prepares participants for diverse roles in SoC design, verification, and emulation projects, enhancing their employability and fostering industry innovation. **Purpose:** ❖ The purpose of A Level chip design program is to equip participants with the necessary skills and knowledge to excel in the field of System-on-Chip (SoC) design, verification, and FPGA emulation	
9.	**Eligibility Criteria for Entry for Student/Trainee/Learner/Employee**	**a. Entry Qualification & Relevant Experience:**	

S. No.	Academic/Skill Qualification (with Specialization - if applicable)	Required Experience (with Specialization - if applicable)
1.	Completed UG Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches	NA
2.	Completed 3 Years of Diploma in Electronics and Communication Engineering/ Electrical	1.5

	Engineering/CS/IT and allied branches after class 10th	
3.	Completed 2nd Year of Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches after class 12th	NA
4.	Acquired NSQF Level 4.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches	1.5 Years
5.	Acquired NSQF Level 4 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches	3 Years

b. Age: 18 years

10. Credits Assigned to this Qualification, Subject to Assessment *(as per National Credit Framework (NCrF))*

26 Credits

11. Common Cost Norm Category (I/II/III) *(wherever applicable)***:**
Category I (Electronics System Design)

12. Any Licensing requirements for Undertaking Training on This Qualification *(wherever applicable)*

NA

13. Training Duration by Modes of Training Delivery *(Specify **Total Duration** as per selected training delivery modes and as per the requirement of the qualification)*

☒ **Offline** ☐ **Online** ☐ **Blended**

Training Delivery Modes	Theory (Hours)	Practical (Hours)	OJT Mandatory (Hours)	ES (Hours)	Total (Hours)
Classroom (offline)	**250**	**350**	**90**	**90**	**780**

**based on the project OJT can be done online/ offline/mixed.*

Training shall be conducted in any of the 3 modes depending on the regional need.

(Refer Blended Learning Annexure-V for details)

14. Aligned to NCO/ISCO Code/s *(if no code is available, mention the same)*

NCO-2015 /2152.0200 (Electronic Engineer)

15. Progression path after attaining the qualification *(Please show Professional and Academic progression)*

Academic:
Advanced courses in SoC Design & Verification, DSP in VLSI, and Analog and Digital IC Design

Professional:
Design/Verification/Application Engineer –> Team Lead –> Project Manager

16. Other Indian languages in which the Qualification & Model Curriculum are being submitted

Qualification file available in English & Hindi Language.

17.	**Is similar Qualification(s) available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No URLs of similar Qualifications:**	
18.	**Is the Job Role Amenable to Persons with Disability**	☒ **Yes** ☐ **No** **If "Yes", specify applicable type of Disability:** a. Locomotor Disability ● Leprosy Cured Person ● Dwarfism ● Muscular Dystrophy ● iv. Acid Attack Victims b. Visual Impairment ● Low Vision	
19.	**How Participation of Women will be Encouraged**	Through funding from the Government under various schemes and projects.	
20.	**Are Greening/ Environment Sustainability Aspects Covered** *(Specify the NOS/Module which covers it)*	☐ **Yes** ☒ **No**	
21.	**Is Qualification Suitable to be Offered in Schools/Colleges**	**Schools** ☐ **Yes** ☒ **No** **Colleges** ☒ **Yes** ☐ **No**	
22.	**Name and Contact Details of Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	**Name:** Jayaraj U Kidav **Email:** jayaraj@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Ishant Kumar Bajpai **Email:** ishant@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Deepam Dubey **Email:** deepamdubey@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Sreejeesh S.G **Email:** sreejeesh@nielit.gov.in **Website:** https://nielit.gov.in/	
23.	**Final Approval Date by NSQC: 30.05.2024**	**24. Validity Duration: 3 Years**	**25. Next Review Date: 30.05.2027**

Section 2: Module Summary

Mandatory NOS/s of Qualifications

- *VLSI Fundamentals*
- *Verilog RTL coding for Synthesis*
- *Static Timing Analysis of VLSI Circuits*
- *FPGA Architecture and Programming*
- *VLSI Verification fundamentals*
- *ASIC Verification using System Verilog and UVM*
- *VLSI Circuits Design for testability*
- *VLSI Physical Design and Verification*
- *Accelerator design using HLS programming*
- *SOC Design and Verification*

Duration and assessment criteria at NOS/ Module level. For further details refer to the curriculum document.

***Th**.-Theory **Pr.**-Practical OJT-On the Job **Man.**-Mandatory Training Rec**.**-Recommended Proj**.**-Project*

S. No	NOS/Module Name	Core/ Non-Core	NOS Code	NCrF/ NSQF Level	Credits as per NCrF	Training Duration (Hours)			Assessment Marks					
						Theory	Practical	Total	Theory	Practical	Proj.	Viva	Total	Weightage (%) *(if applicable)*
1.	*NOS1:* VLSI Fundamentals	Core	NIE/ELE /N0101	4	2	25	35	60	100	80	-	20	200	9.3
2.	*NOS2:* Verilog RTL coding for Synthesis	Core	NIE/ELE /N0102	4	2	25	35	60	100	80	-	20	200	9.3
3.	*NOS3:* Static Timing Analysis of VLSI Circuits	Core	NIE/ELE /N0103	4	2	25	35	60	100	80	-	20	200	9.3
4.	NOS4: FPGA Architecture and Programming	Core	NIE/ELE /N0104	4	2	25	35	60	100	80	-	20	200	9.3
5.	NOS5: VLSI Verification fundamentals	Core	NIE/ELE /N0105	5	2	25	35	60	100	80	-	20	200	9.3

S. No	NOS/Module Name	Core/ Non-Core	NOS Code	NCrF/ NSQF Level	Credits as per NCrF	Training Duration (Hours)			Assessment Marks					
						Theory	Practical	Total	Theory	Practical	Proj.	Viva	Total	Weightage (%) *(if applicable)*
6.	NOS6: ASIC Verification using System Verilog and UVM	Core	NIE/ELE/N0106	5	2	25	35	60	100	80	-	20	200	9.3
7.	NOS7: VLSI Circuits Design for testability	Core	NIE/ELE/N0107	5	2	25	35	60	100	80	-	20	200	9.3
8.	NOS 8: VLSI Physical Design and Verification	Core	NIE/ELE/N0108	5	2	25	35	60	100	80	-	20	200	9.3
9.	NOS 9: Accelerator design using HLS programming	Core	NIE/ELE/N0109	5	2	25	35	60	100	80	-	20	200	9.3
10.	NOS 10: SOC Design and Verification	Core	NIE/ELE/N0110	5	2	25	35	60	100	80	-	20	200	9.3
11.	NOS 11: Employability Skill	Non-Core	DGT/VSQ/N0103	5	3	0	0	90	-	-	-	-	50	2
12.	NOS12: OJT/Project	Core	NIE/ELE/N0111	5	3	0	0	90	-	-	80	20	100	5
Duration (in Hours) / Total Marks					**26**	**250**	**350**	**780**	**1000**	**800**	**80**	**220**	**2150**	**100**

Assessment Components	NOS Included	Duration* (in mins)	Marks
Theory Paper 1 – VLSI Fundamentals	1	90	100
Theory Paper 2 – Verilog RTL coding for Synthesis	2	90	100
Theory Paper 3– Static Timing Analysis of VLSI Circuits	3	90	100
Theory Paper 4 – FPGA Architecture and Programming	4	90	100
Theory Paper 5– VLSI Verification fundamentals	5	90	100
Theory Paper 6– ASIC Verification using System Verilog and UVM	6	90	100
Theory Paper 7– VLSI Circuits Design for testability	7	90	100
Theory Paper 8 – VLSI Physical Design and Verification	8	90	100
Theory Paper 9– Accelerator design using HLS programming	9	90	100
Theory Paper 10 – SOC Design and Verification	10	90	100
Practical Paper 1– VLSI Fundamentals	1	180	100
Practical Paper 2– Verilog RTL coding for Synthesis	2	180	100
Practical Paper 3– Static Timing Analysis of VLSI Circuits	3	180	100
Practical Paper 4 – FPGA Architecture and Programming	4	180	100
Practical Paper 5– VLSI Verification fundamentals	5	180	100
Practical Paper 6– ASIC Verification using System Verilog and UVM	6	180	100
Practical Paper 7– VLSI Circuits Design for testability	7	180	100
Practical Paper 8 – VLSI Physical Design and Verification	8	180	100
Practical Paper 9– Accelerator design using HLS programming	9	180	100
Practical Paper 10 – SOC Design and Verification	10	180	100
NOS11: Employability Skills	11		50
NOS12: OJT/Project	1,2,3,4,5,6,7,8, 9,10		100
		Grand Total	**2150**

*** Assessment Strategy shall be as per NIELIT Norms prevailing at times.**

Minimum Pass Percentage – The pass percentage is 50% in each assessment component (as mentioned in the above table) with the aggregate pass percentage be 50%

Section 3: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI
3.	**Tools and Equipment Required for Training**	☒Yes ☐No (*If "Yes", details to be provided in Annexure)* *Details available in Annexure II*
4.	**In Case of Revised Qualification, Details of Any Upskilling Required for Trainer**	Nil

Section 4: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B.E/B. Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech
4.	**Assessment Mode** *(Specify the assessment mode)*	Online for Theory Online/ Offline/ Blended for other assessment components depending on the region where the assessment is conducted

5.	**Tools and Equipment Required for Assessment**	☒ Same as for training ☒ Yes ☐ No (*Details to be provided in Annexure-II)*

Section 5: Evidence of the need for the Qualification

Provide Annexure/Supporting documents name.

1.	**Latest Skill Gap Study (not older than 2 years) (Yes/No):** Yes, Available in Annexure-A: Evidence of Need
2.	**Latest Market Research Reports or any other source (not older than 2 years) (Yes/No):** Yes, Available at Annexure-A: Evidence of Need
3.	**Government /Industry initiatives/ requirement (Yes/No):** Yes, Available at Annexure-A: Evidence of Need
4.	**Number of Industry validation provided:** 7
5.	**Estimated no. of persons to be trained and employed:** 500 persons per year shall be trained.
6.	**Evidence of Concurrence/Consultation with Line Ministry/State Departments:** NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.

Section 6: Annexure & Supporting Documents Checklist

1.	**Annexure:** NCrF/NSQF level justification based on NCrF level/NSQF descriptors *(Mandatory)*	Available at Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for qualification *(Mandatory, except in case of online course)*	*Available at Annexure-II: Tools and Equipment*
3.	**Annexure:** Detailed Assessment Criteria *(Mandatory)*	*Available at Annexure-VI: Detailed Assessment Criteria*
4.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at Annexure-VII: Detailed Assessment Strategy*
5.	**Annexure:** Blended Learning *(Mandatory, in case selected Mode of delivery is "Blended Learning")*	*Available at Annexure-V: Blended Learning*
6.	**Annexure:** Industry Validation Summary	*Available at Annexure-III: Industry Validation* *The copy is available at Annexure-B*
7.	**Annexure:** Multiple Entry-Exit Details *(Mandatory, in case qualification has multiple Entry-Exit)*	*NA*
8.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at Annexure-IX: Acronym and Glossary*
9.	**Supporting Document:** Model Curriculum *(Mandatory – Public view)*	*Available at Annexure-C: Model Curriculum*

10.	**Supporting Document:** Occupational Map *(Mandatory)*	*Available at Annexure-VIII: Occupational Map*
11.	**Any other document you wish to submit:**	*Annexure-D: Examination SoP*

Annexure I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	Theoretical and practical knowledge in implementation of VLSI Design and Verification	Requires a command of wide-ranging specialised theoretical and practical skills, involving variable routine and non-routine contexts.	5
Professional and Technical Skills/ Expertise/ Professional Knowledge	Theoretical knowledge in VLSI Design and Verification using FPGA prototyping, Physical design, SoC Design and Verification	Wide-ranging factual and theoretical knowledge in broad contexts within a field of work or study.	5
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	Ability to prototype algorithms on FPGA and implement them in full IC design and Verification flow	Wide range of cognitive and practical skills required to generate solutions to specific problems in a field of work of study.	5
Broad Learning Outcomes/Core Skill	Ability to independently develop the logic required for performing the VLSI Design and verification tasks	Good logical and mathematical skill understanding of social political and natural environment and organising information, communication and presentation skill.	5
Responsibility	Ability to manage the system resources most effectively by appropriate planning, estimation, coordination and control of the activities involved in the design & development of any task/project	Full responsibility for output of group and development	5

Annexure II: Tools and Equipment (Lab Set-Up)

LIST OF EQUIPMENT (For a batch of 30 students)

Description		Qty	Specifications
1	Classroom	1	30 Sq.m

2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Annexure III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
2	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
3	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
4	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba, Medinipur	9434996748	bginfotech2007@gmail.com

5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com
6	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com
7	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com

Annexure IV: Training & Employment Details

Training and Employment Projections:

Year	Total Candidates		Women		People with Disability	
	Estimated Training #	Estimated Employment Opportunities	Estimated Training #	Estimated Employment Opportunities	Estimated Training #	Estimated Employment Opportunities
2024	500	200	200	100	25	10
2025	750	350	350	150	50	20
2026	750	350	350	150	50	20

Data to be provided year-wise for next 3 years

Training, Assessment, Certification, and Placement Data for previous versions of qualifications: NA

List Schemes in which the previous version of Qualification was implemented: NA

Content availability for previous versions of qualifications:

☐ Participant Handbook ☐ Facilitator Guide ☒ Digital Content ☐ Qualification Handbook

Languages in which Content is available: English

Annexure V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	☐Theory/ Lectures - Imparting theoretical and	Online interaction platforms like JitSi Meet, Bharat VC, Google	20:80

	conceptual knowledge	Meet, MS Teams, etc.	
2	☐Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
3	☐Showing Practical Demonstrations to the learners	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
4	☐Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
5	☐Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
6	☐Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	☐On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Design Software	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure VI: Detailed Assessment Criteria

Detailed assessment criteria for each NOS/Module are as follows:

NOS/Module Name	Assessment Criteria for Performance Criteria/Learning Outcomes	Theory Marks	Practical Marks	Project Marks	Assignment Marks
NOS1: VLSI Fundamentals	Introduction to VLSI Design & CMOS Transistor Theory	25	20	-	5
	CMOS Inverter Characteristics and Logic Design	25	20	-	5
	Transistor Schematic, Layouts & On-chip wire modelling	25	20	-	5
	Gate Delay, Logical Effort, Critical Path Optimization and Timing analysis for Sequential circuits	25	20	-	5
	Total Marks	**100**	**80**	**-**	**20**
NOS2: Verilog RTL coding for Synthesis	RTL Design Methodology	25	20	-	5
	Digital Logic Design Principles	25	20	-	5
	RTL Design Using HDL	25	20	-	5
	RTL Simulation and Verification	25	20	-	5
	Total Marks	**100**	**80**	**-**	**20**

NOS3: Static Timing Analysis of VLSI Circuits	Overview of VLSI STA	30	25	-	6
	Timing performance	30	25	-	7
	STA using EDA tools	40	30	-	7
	Total Marks	**100**	**80**	**-**	**20**
NOS4: FPGA Architecture and Programming	Introduction to FPGAs	25	20	-	5
	Hardware Description Languages for FPGAs	25	20	-	5
	FPGA Design Flow and Optimization Technique	25	20	-	5
	FPGA Verification and Debugging	25	20	-	5
	Total Marks	**100**	**80**	**-**	**20**
NOS5: VLSI Verification fundamentals	Basics of Verilog HDL for verification	25	20	-	5
	Hierarchal Modeling and test benching for verification	25	20	-	5
	Introduction to Verification, Verification Types, Verification Architecture and Flow	25	20	-	5
	Test Automation and Scripting	25	20	-	5
	Total Marks	**100**	**80**	**-**	**20**
NOS6: ASIC Verification using System Verilog and UVM	Integrated Circuit verification.	30	25	-	6
	Processor Architecture and Processor verification, SoC Verification	30	25	-	7
	Methodology based SoC Verification, SoC Emulation and post silicon Validation	40	30	-	7
	Total Marks	**100**	**80**	**-**	**20**
NOS7: VLSI Circuits Design for testability	Overview of DFT for VLSI	30	25	-	6
	ATPG and BIST	30	25	-	7
	JTAG and IJTAG	40	30	-	7
	Total Marks	**100**	**80**	**-**	**20**
NOS8: VLSI Physical Design and Verification	Introduction to Physical Design ,VLSI Physical Design Flow	30	25	-	6
	Verification Techniques	30	25	-	7
	Design Tools and EDA	40	30	-	7
	Total Marks	**100**	**80**	**-**	**20**
NOS9: Accelerator design using HLS programming	Combination Circuits and Test Benches using C/C++	30	25	-	6
	Sequential Circuits Design using HLS	30	25	-	7
	Function Acceleration on FPGA	40	30	-	7
	Total Marks	**100**	**80**	**-**	**20**
NOS10: SOC Design and Verification	Advanced SoCs and methodology based SoC Verification	30	25	-	6

	SoC Emulation and Post silicon verification and validation	30	25	-	7
	High level synthesis	40	30	-	7
	Total Marks	**100**	**80**	**-**	**20**
NOS11: Employability Skills	Employability Skills	0	0	0	50
NOS12: Project / OJT	Project	0	0	80	20
	Grand Total-2150	**1000**	**800**	**80**	**270**

Annexure VII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria. The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. Competence acquired by the candidate can be obtained by conducting Theory (Online), Practical assessment, internal assessment, Project/Presentation/ Assignment, Major Project. The emphasis is on the practical demonstration of skills & knowledge gained by the candidate through the training. Each OUTCOME is assessed & marked separately. A candidate is required to pass all OUTCOMES individually based on the passing criteria.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.
2. The assessor assigns the roll number.
3. The assessor carries out theory online assessments through remote proctoring methodology. Theory examination would be conducted online and the paper comprise of MCQ. Conduct of assessment are through trained proctors. Once the test begins, remote proctors have full access to candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I- card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
4. An External Examiner/ Observer may be deployed including NIELIT officials for evaluation of Practical examination/ internal assessment / Project/ Presentation/. Major Project (if applicable) would be evaluated preferably by external/ subject expert including NIELIT officials.

5. Pass percentage would be 50% marks in each component.
6. Candidates may apply for re-examination within the validity of registration (only in the assessment component in which the candidate failed).
7. For re-examination prescribed examination fee is required to be paid by the candidate only for the assessment component in which the candidate wants to reappear.
8. There would be no exemption for any paper/module for candidates having similar qualifications or skills.
9. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-VIII: Occupational Map

Enclosed separately with this QF

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
ISCO	International Standard Classification of Occupations
NCO	National Classification of Occupations
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework
OJT	On the Job Training

Glossary

Term	Description
National Occupational Standards (NOS)	NOS defines the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.
Long Term Training	Long-term skilling means any vocational training program undertaken for a year and above. https://ncvet.gov.in/sites/default/files/NCVET.pdf