QUALIFICATION FILE – Standalone NOS

Fundamentals of Design for Testability for VLSI Circuits

☐ Horizontal/Generic ☐ Vertical/Specialization

☒ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☒ OEM

NCrF/NSQF Level: 5

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY

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Table of Contents

Section 1: Basic Details

1.	**NOS-Qualification Name**	**Fundamentals of Design for Testability for VLSI Circuits**	
2.	**Sector/s**	Electronics	
3.	**Type of Qualification ☒New ☐ Revised**	**NQR Code & version of the existing /previous qualification: NA**	**Qualification Name of the existing/previous version: NA**
4.	**National Qualification Register (NQR) Code & Version** *(Will be issued after NSQC approval.)*	NG-05-EH-02907-2024-V1-NIELIT	**5. NCrF/NSQF Level: 5**
6.	**Brief Description of the Standalone NOS**	The standalone (NOS) focuses on comprehensive testing and fault detection. It includes Design for Test (DFT) strategies to identify manufacturing faults and design defects, utilizing Scan ATPG and Fault Simulation techniques for thorough verification. Key testing modes such as BIST (Built-In Self-Test), MBIST (Memory BIST), and LBIST (Logic BIST) autonomously test circuit components. Boundary Scan technology ensures robust testing of interconnected circuits using specific cells and instructions. Integration with JTAG and IJTAG standards provides standardized interfaces and procedural languages for efficient testing and control. Overall, the standalone NOS enhances VLSI design reliability and manufacturability through advanced testing methodologies and standardized frameworks.	
7.	**Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee**	**a. Entry Qualification & Relevant Experience:**	

S. No.	Academic/Skill Qualification (with Specialization - if applicable)	Relevant Experience (with Specialization - if applicable)
1	2nd year of UG in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	NA
2	3 Years of Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 10th	1.5 Years

3	2 Year of diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 12th	NA
4	NSQF Level 4.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years
5	NSQF Level 4 Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years

b. Age: 18 Years

8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	2 Credits	**9. Common Cost Norm Category (I/II/III)** *(wherever applicable)***:** Category-I
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA	
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☒**Offline** ☐ **Online** ☐ **Blended**	

Training Delivery Mode	Theory (Hours)	Practical (Hours)	Total (Hours)
Classroom (offline)	30	30	60

The mode of delivery shall be based on the regional demand and can be offered in anyof the above modes mentioned.

<table>
<tr><td>12.</td><td>Assessment Criteria</td><td>
<table>
<tr><th>Theory (Marks)</th><th>Practical (Marks)</th><th>Project/ Presentation /Assignment (Marks)</th><th>Viva/ Internal Assessment (Marks)</th><th>Total (Marks)</th></tr>
<tr><td>100</td><td>60</td><td>20</td><td>20</td><td>200</td></tr>
</table>
The centralized online assessment is conducted by the Examination Wing, NIELIT Headquarters.
</td></tr>
<tr><td>13.</td><td>Is the NOS Amenable to Persons with Disability</td><td>☒ Yes ☐ No If “Yes”, specify applicable type of Disability:
a) Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims
b) Visual Impairment: Low Vision</td></tr>
<tr><td>14.</td><td>Progression Path After Attaining the Qualification, wherever applicable (Please show Professional and Academic progression)</td><td>Design Engineer->Application Engineer->Team Lead -> Project Manager</td></tr>
<tr><td>15.</td><td>How participation of women will be encouraged?</td><td>Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women’s participation under other schemes launched by the Government from time to time.</td></tr>
<tr><td>16.</td><td>Other Indian languages in which the Qualification & Model Curriculum are being submitted</td><td>Qualification files available in English & Hindi Language</td></tr>
<tr><td>17.</td><td>Is similar NOS available on NQR-if yes, justification for this qualification</td><td>☐ Yes ☒ No URLs of similar Qualifications:</td></tr>
<tr><td>18.</td><td>Name and Contact Details Submitting / Awarding Body SPOC
(In case of CS or MS, provide details of both Lead AB & Supporting ABs)</td><td>Name: Jayaraj U Kidav
Email: jayaraj@nielit.gov.in
Website: https://nielit.gov.in/
Name: Ishant Kumar Bajpai
Email: ishant@nielit.gov.in
Website: https://nielit.gov.in/
Name: Deepam Dubey
Email: deepamdubey@nielit.gov.in
Website: https://nielit.gov.in/</td></tr>
</table>

		Name: Sreejeesh S.G Email: sreejeesh@nielit.gov.in Website: https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI Design
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI Design
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No Available at Annexure-II
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B. Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on

		registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech.
4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted
5.	**Tools and Equipment Required for Assessment**	Same as for training ☒ Yes ☐ No

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided: 7
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure:** Industry Validation	*Available at* Annexure-III: Industry Validation
4.	**Annexure:** Training Details	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning
6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	• In-depth knowledge of Design for Test (DFT) techniques, including fault simulation, ATPG, and scan test design rules, to ensure effective detection of manufacturing defects and transition delays in digital designs. • Theoretical grasp of MBIST and LBIST mechanisms, including their control modes and implementation processes, to validate and test complex VLSI systems reliably. • Detailed understanding of JTAG TAP registers, IJTAG concepts like Segment Insertion Bit (SIB), Instrument Connectivity Language (ICL), and Procedural Description Language (PDL) for scalable and efficient instrumentation and testing.	• The above job role requires a deep understanding of DFT methodologies, enabling professionals to apply fault simulation, ATPG, and scan tests to identify and rectify design defects effectively. • Mastery of BIST techniques, including MBIST and LBIST, equips candidates to ensure robust validation of complex VLSI systems. Additionally, proficiency in JTAG and IJTAG protocols supports scalable and automated testing, critical for maintaining high-quality design standards in industrial applications.	5
Professional and Technical Skills/ Expertise/ Professional Knowledge	• Proficiency in implementing Design for Testability (DFT) techniques, including Scan Insertion, ATPG generation, fault simulation, and transition delay testing, to ensure efficient and reliable VLSI testing processes. • Advanced knowledge of Built-In Self-Test (BIST) mechanisms such as MBIST, LBIST, and boundary scan techniques to design and validate test architectures for complex VLSI systems. • Competence in understanding and applying JTAG/IJTAG protocols, including handling Test Access Ports (TAP), configuring Segment Insertion Bits (SIB), and utilizing Instrument Connectivity	• The job role emphasizes expertise in DFT methodologies, equipping candidates to perform scan insertion, ATPG, and fault simulation for ensuring robust VLSI testing. • Proficiency in BIST and boundary scan techniques enables the design and validation of self-testing mechanisms for complex chip architectures. Mastery of JTAG/IJTAG protocols ensures the capability to implement scalable, automated testing solutions critical for advancing VLSI design and validation processes.	5

	Language (ICL) and Procedural Description Language (PDL) for scalable and automated testing solutions.		
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	• Candidates must demonstrate a strong understanding of DFT methodologies, including ATPG, fault simulation, and scan test for detecting transition delays. This ensures readiness to implement efficient testing processes in industrial scenarios or entrepreneurial projects. • Knowledge of BIST (MBIST, LBIST) and Boundary Scan techniques equips candidates to design and validate complex VLSI systems independently, enhancing their ability to contribute to innovative testing solutions and develop proprietary testing frameworks. • Mastery of JTAG and IJTAG protocols, including handling TAP registers and leveraging ICL/PDL for instrumentation, prepares candidates to develop scalable and automated test solutions, critical for both employment in advanced VLSI testing roles and entrepreneurship in chip design validation.	• The job role emphasizes taking ownership of the verification and validation processes to ensure ICs, processors, and SoCs meet functional and quality standards. • It involves responsibility for implementing advanced methodologies like UVM and ABV, ensuring the reliability and compliance of designs. Managing end-to-end verification, from simulation to post-silicon validation, reflects accountability for delivering error-free, optimized embedded systems	5
Broad Learning Outcomes/Core Skill	• Demonstrate the ability to identify manufacturing faults and apply design-for-test strategies, including scan design and transition delay testing, to ensure high-quality VLSI systems. • Exhibit competence in utilizing ATPG, BIST (MBIST, LBIST), and boundary scan methods for efficient fault detection and validation of integrated circuits. • Skillfully manage test access ports, TAP registers, and implement scalable testing frameworks using ICL and PDL to address modern VLSI design challenges.	• The job role focuses on developing core skills by enabling a deep understanding of DFT principles, ensuring candidates can address manufacturing defects and implement efficient testing methodologies. • Proficiency in advanced techniques like ATPG, BIST, and boundary scan enhances fault detection capabilities critical for quality assurance. • Mastery of JTAG/IJTAG protocols equips individuals with the technical expertise to	5

		develop scalable and automated solutions, aligning with industry standards and fostering innovation.	
Responsibility	• Candidates must demonstrate accountability in implementing DFT techniques, such as ATPG, BIST, and fault simulation, ensuring the accuracy and reliability of VLSI designs in industrial applications. • Professionals must ensure compliance with industry protocols, such as JTAG/IJTAG, and maintain quality benchmarks in testing, debug processes, and hardware validation. • Candidates should take ownership of optimizing testing flows, scan insertion methodologies, and boundary scan implementations to enhance system validation and reduce production defects.	• The job role emphasizes accountability in implementing robust DFT techniques like ATPG, BIST, and fault simulation to ensure VLSI design reliability and fault coverage. • It requires strict adherence to industry testing protocols, including JTAG/IJTAG, to maintain quality and compliance in validation processes. • Professionals are expected to take responsibility for optimizing testing methodologies, driving efficiency, and minimizing defects during production and deployment.	5

Annexure-II: Tools and Equipment (lab set-up)

LIST OF EQUIPMENT (For a batch of 30 students)

	Description	Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	

5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
2	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
3	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
4	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba,	9434996748	bginfotech2007@gmail.com

				Medinipur		
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com
6	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com
7	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2024-25	500	200	20
2025-26	500	200	20
2026-27	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	☐Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80

2	☐Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
3	☐Showing Practical Demonstrations to the learners	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
4	☐Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
5	☐Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
6	☐Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	☐On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Design Software	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. **Description:**

The syllabus provides a comprehensive exploration of Design for Test (DFT) in VLSI circuits, covering fundamental concepts such as the importance and implementation of DFT principles for detecting manufacturing faults and design defects essential for circuit reliability. It includes detailed studies on Built-In Self-Test (BIST) methodologies like Memory BIST (MBIST) and Logic BIST (LBIST), alongside Automatic Test Pattern Generation (ATPG) techniques for efficient fault detection.

2. Scope:

The scope covers the following:

This NOS Covers essential concepts such as the role of DFT in identifying manufacturing faults and design defects, emphasizing the necessity of testing in ensuring circuit reliability, delving into ATPG methodologies including BIST (Built-In Self-Test), MBIST (Memory BIST), and LBIST (Logic BIST), alongside Boundary Scan techniques for comprehensive testing coverage. Exploring DFT compiler workflows and scan insertion flows for efficient test pattern generation. JTAG for external testing through Registers and the Test Access Port (TAP), and IJTAG for internal testing with features like Segment Insertion Bit (SIB), Instrument Connectivity Language (ICL), and Procedural Description Language (PDL), crucial for intricate test strategy implementations in VLSI circuits.

3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

Overview of DFT for VLSI

- Understand the fundamentals of Design for Test (DFT), including the identification of manufacturing faults and design defects.
- Demonstrate proficiency in Scan ATPG (Automatic Test Pattern Generation) and fault simulation techniques.
- Apply scan design rules and conduct scan tests focusing on transition delays.

ATPG and BIST

- Implement Built-In Self-Test (BIST) techniques, including MBIST (Memory BIST) and LBIST (Logic BIST).
- Utilize Boundary Scan techniques for testing and debugging using Boundary Scan Cells and Instructions.
- Execute flows supported by DFT compilers for scan insertion and manage DFT compiler flows and commands proficiently.

JTAG and IJTAG

- Describe the JTAG standard and its components, including Registers and the Test Access Port (TAP).
- Implement IJTAG for internal component testing, utilizing Segment Insertion Bit (SIB) functionalities.
- Script and automate test procedures using Procedural Description Language (PDL) in IJTAG environments for efficient testing and validation.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Gain expertise in Design for Test (DFT), essential for identifying manufacturing faults and design defects in VLSI circuits, employing methods like Scan ATPG, Fault Simulation, and scan design rules to ensure thorough testing, including targeting transition delays.
- Develop comprehensive skills in Built-In Self-Test (BIST), covering MBIST and LBIST methodologies for efficient memory and logic testing. Additionally, master Boundary Scan techniques integrated into DFT workflows via DFT compilers, alongside proficiency in scan insertion flows and command utilization.
- Become proficient in JTAG fundamentals, emphasizing Registers and the Test Access Port (TAP) for external testing. Explore Internal JTAG (IJTAG) capabilities for internal component testing in VLSI circuits. Master the use of Instrument Connectivity Language (ICL) and Procedural Description Language (PDL) for configuring test instruments and automating test procedures in IJTAG environments.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1. Understanding fundamental principles of Design for Test (DFT), including identifying manufacturing faults, design defects, and the necessity of testing for ensuring VLSI circuit reliability and performance.

GS2. Proficiency in Scan-based Automatic Test Pattern Generation (ATPG) and Built-In Self-Test (BIST) methodologies (MBIST, LBIST), essential for comprehensive memory and logic testing.

GS3. Ability to integrate Boundary Scan techniques into DFT workflows using DFT compilers, along with mastery of scan insertion flows and command usage within DFT compiler environments.

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project Marks	Viva Marks
Fundamentals of Design for Testability for VLSI Circuits	**Overview of DFT for VLSI**	30	20	-	6
	● Understand the fundamentals of Design for Test (DFT), including the identification of manufacturing faults and design defects.	-	-	-	-
	● Demonstrate proficiency in Scan ATPG (Automatic Test Pattern Generation) and fault simulation techniques.	-	-	-	-
	● Apply scan design rules and conduct scan tests focusing on transition delays.	-	-	-	-
	ATPG and BIST	30	20	-	7
	● Implement Built-In Self-Test (BIST) techniques, including MBIST (Memory BIST) and LBIST (Logic BIST).	-	-	-	-
	● Utilize Boundary Scan techniques for testing and debugging using Boundary Scan Cells and Instructions.	-	-	-	-
	● Execute flows supported by DFT compilers for scan insertion and manage DFT compiler flows and commands proficiently.	-	-	-	-
	JTAG and IJTAG	40	20	-	7
	● Describe the JTAG standard and its components, including Registers and the Test Access Port (TAP).	-	-	-	-
	● Implement IJTAG for internal component testing, utilizing Segment Insertion Bit (SIB) functionalities.	-	-	-	-
	● Script and automate test procedures using Procedural Description Language (PDL) in IJTAG environments for efficient testing and validation.	-	-	-	-
	Total Marks -200	**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym:

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary:

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.