QUALIFICATION FILE – Standalone NOS

Fundamentals of VLSI Physical Design and Verification

☐ Horizontal/Generic ☐ Vertical/Specialization

☒ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒Future Skills ☒ OEM

NCrF/NSQF Level: 5

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

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Table of Contents

Section 1: Basic Details

<table>
<tr><td>1.</td><td>NOS-Qualification Name</td><td colspan="2">Fundamentals of VLSI Physical Design and Verification</td></tr>
<tr><td>2.</td><td>Sector/s</td><td colspan="2">Electronics</td></tr>
<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version (Will be issued after NSQC approval.)</td><td>NG-05-EH-02908-2024-V1-NIELIT</td><td>5. NCrF/NSQF Level: 5</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">The standalone (NOS) in VLSI Physical Design and Verification provides essential tools and methodologies for implementing and understanding the physical design and verification of integrated circuits. It guides through the entire VLSI design flow, from RTL (Register Transfer Level) to GDSII (Graphic Data System II), focusing on industry-standard techniques and fabrication technologies such as CMOS and photolithography.
Key areas covered include logic synthesis, placement, routing, and power management, alongside verification methods like functional simulation, static timing analysis, and layout versus schematic (LVS) checks. Electronic Design Automation (EDA) tools are pivotal, supporting tasks such as place and route, simulation, and comprehensive verification. Real-world case studies illustrate design challenges, optimization strategies, and career paths in the dynamic field of VLSI design and verification.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
<table>
<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Relevant Experience (with Specialization - if applicable)</th></tr>
<tr><td>1</td><td>2nd year of UG in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches</td><td>NA</td></tr>
<tr><td>2</td><td>3 Years of Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics</td><td>1.5 Years</td></tr>
</table></td></tr>
</table>

			and allied branches after class 10th	
		3	2 Year of diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 12th	NA
		4	NSQF Level 4.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years
		5	NSQF Level 4 Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years
		b. Age: 18 Years		
8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	2 Credits	**9. Common Cost Norm Category (I/II/III)** *(wherever applicable)*: Category-I	
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA		
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☒ **Offline** ☐ **Online** ☐ **Blended**		

Training Delivery Mode	**Theory (Hours)**	**Practical (Hours)**	**Total (Hours)**
Classroom (offline)	30	30	60

The mode of delivery shall be based on the regional demand and can be offered in anyof the above modes mentioned.

<table>
<tr><td>12.</td><td>Assessment Criteria</td><td>
<table>
<tr><th>Theory (Marks)</th><th>Practical (Marks)</th><th>Project/ Presentation /Assignment (Marks)</th><th>Viva/ Internal Assessment (Marks)</th><th>Total (Marks)</th><th>Passing %age</th></tr>
<tr><td>100</td><td>60</td><td>20</td><td>20</td><td>200</td><td>50%</td></tr>
</table>
The centralized online assessment is conducted by the Examination Wing, NIELIT Headquarters.
</td></tr>
<tr><td>13.</td><td>Is the NOS Amenable to Persons with Disability</td><td>☒ Yes ☐ No If “Yes”, specify applicable type of Disability:
a) Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims
b) Visual Impairment: Low Vision</td></tr>
<tr><td>14.</td><td>Progression Path After Attaining the Qualification, wherever applicable (Please show Professional and Academic progression)</td><td>Design/Application Engineer/Team Lead / Project Manager</td></tr>
<tr><td>15.</td><td>How participation of women will be encouraged?</td><td>Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women’s participation under other schemes launched by the Government from time to time.</td></tr>
<tr><td>16.</td><td>Other Indian languages in which the Qualification & Model Curriculum are being submitted</td><td>Qualification files available in English & Hindi Language</td></tr>
<tr><td>17.</td><td>Is similar NOS available on NQR-if yes, justification for this qualification</td><td>☐ Yes ☒ No URLs of similar Qualifications:</td></tr>
<tr><td>18.</td><td>Name and Contact Details Submitting / Awarding Body SPOC
(In case of CS or MS, provide details of both Lead AB & Supporting ABs)</td><td>Name: Jayaraj U Kidav
Email: jayaraj@nielit.gov.in
Website: https://nielit.gov.in/
Name: Ishant Kumar Bajpai
Email: ishant@nielit.gov.in
Website: https://nielit.gov.in/
Name: Deepam Dubey
Email: deepamdubey@nielit.gov.in
Website: https://nielit.gov.in/
Name: Sreejeesh S.G</td></tr>
</table>

		Email: sreejeesh@nielit.gov.in Website: https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI Design
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI Design
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No Available at Annexure-II
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B. Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on

		registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech.
4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted
5.	**Tools and Equipment Required for Assessment**	Same as for training ☒ Yes ☐ No

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided: 7
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure:** Industry Validation	*Available at* Annexure-III: Industry Validation
4.	**Annexure:** Training Details	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning
6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/ NSQF Level
Professional Theoretical Knowledge/Process	• Knowledge of the physical design process from RTL to GDSII, including placement, routing, clock tree synthesis, and power planning, ensures theoretical preparedness for tackling real-world chip design challenges. • Mastery of functional, timing, and power integrity verification processes, such as static timing analysis and layout-vs-schematic (LVS) checks, is critical for ensuring design reliability and performance. • Theoretical knowledge of CMOS technology, photolithography, and fabrication techniques provides foundational insights into how design translates into physical devices, ensuring compatibility and manufacturability.	• Professionals are expected to understand verification processes like functional simulation, static timing analysis, and signal integrity checks, ensuring designs meet performance and reliability criteria. • Familiarity with electronic design automation tools, their workflows, and practical case studies bridges theoretical knowledge and its application in solving complex design challenges, critical for advancing in VLSI development roles.	5
Professional and Technical Skills/ Expertise/ Professional Knowledge	• Demonstrated expertise in performing physical design tasks such as floorplanning, cell placement, clock tree synthesis, and routing using industry-standard EDA tools, while optimizing for power, performance, and area. • Strong ability to conduct functional verification, timing analysis, and power integrity checks, ensuring designs are error-free and meet all specifications, with the capability to debug and resolve complex issues effectively. • Proficient in utilizing simulation, layout editing, and verification tools, including Verilog/VHDL simulators and LVS checkers, coupled with the ability to analyze and optimize real-world chip layouts for performance	• The job role requires strong proficiency in physical design processes, including floorplanning, placement, and routing, using industry-standard EDA tools to optimize for power, performance, and area. It emphasizes expertise in verification techniques, such as functional, timing, and power integrity analysis, to ensure design compliance and reliability. • Additionally, professionals must be adept at analyzing chip layouts and leveraging advanced tools for debugging, validation, and design optimization, reflecting technical excellence and problem-solving abilities.	5

	improvements.		
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	• Candidates must demonstrate the ability to implement VLSI physical design flows, including placement, routing, clock tree synthesis, and power planning, using industry-standard EDA tools. This ensures readiness for roles in chip design and optimization or entrepreneurial ventures in custom IC design. • The ability to perform functional and timing verification, handle signal integrity challenges like IR drop and crosstalk, and conduct Layout vs. Schematic (LVS) checks equips candidates to ensure design reliability and compliance, essential for employment or launching design validation services. • Understanding case studies and optimizing chip layouts prepares candidates to tackle design complexities, improve performance, and innovate, enabling them to contribute effectively to high-performance chip development or establish a niche in customized IC solutions.	• The job role equips candidates with industry-ready skills in VLSI physical design and verification, enabling immediate contribution to cutting-edge semiconductor projects. • It fosters an entrepreneurial mindset by preparing professionals to innovate and optimize chip designs, addressing power, performance, and cost challenges in niche markets.	5
Broad Learning Outcomes/Core Skill	• The ability to analyze and optimize VLSI designs for efficient placement, routing, and clock tree synthesis while addressing power and timing constraints demonstrates strong critical thinking and adaptability. • Hands-on expertise in industry-standard EDA tools for design, simulation, and verification supports core skills in navigating the complexities of VLSI design environments. • Applying precision in functional, timing, and power integrity verification processes ensures high-quality outcomes and enhances reliability, a fundamental requirement in VLSI design projects.	• The job role aligns with broad learning outcomes by fostering critical analytical skills necessary to optimize VLSI designs for placement, routing, and power management. • Proficiency in using industry-standard EDA tools strengthens the foundational technical expertise required for tackling complex design environments. Additionally, the focus on precision in verification and validation ensures the development of reliable and high-quality VLSI systems, reflecting attention to detail and problem-solving acumen.	5

Responsibility	• Ensure precise execution of VLSI physical design processes, including floorplanning, placement, and routing, while adhering to industry standards and project specifications. • Take responsibility for verifying functional, timing, and power integrity through rigorous testing methodologies, including static timing analysis and IR drop analysis. • Oversee the end-to-end design flow from RTL to GDSII, ensuring optimal power, performance, and area trade-offs while meeting project timelines and deliverables.	• The job role emphasizes ownership and accountability in executing VLSI physical design tasks, ensuring adherence to industry standards and project requirements. Professionals must take responsibility for quality assurance, verifying design accuracy and optimizing functional, timing, and power parameters through robust testing.	5

Annexure-II: Tools and Equipment (lab set-up)

LIST OF EQUIPMENT (For a batch of 30 students)

	Description	Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent

			Memory: 16GB RAM, Internal Storage: 500GB Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
2	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
3	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
4	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba, Medinipur	9434996748	bginfotech2007@gmail.com
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com

6	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com
7	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2024-25	500	200	20
2025-26	500	200	20
2026-27	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	☐Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
2	☐Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80

3	☐Showing Practical Demonstrations to the learners	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
4	☐Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
5	☐Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
6	☐Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	☐On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Design Software	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. Description:

The syllabus provides a thorough introduction to VLSI physical design, covering foundational concepts and the industry-standard design flow. It explores CMOS technology and photolithography as fundamental to the fabrication process. Students will learn the entire VLSI physical design flow, from RTL design and synthesis to placement and routing, emphasizing floorplanning, cell placement, and clock tree synthesis.

2. Scope:

The scope covers the following:

- The scope of this course encompasses the entire VLSI physical design process, from RTL coding to final chip layout (GDSII). It covers key topics such as CMOS fabrication, design flow, placement, routing, power planning, and clock tree synthesis. Additionally, students will gain hands-on experience with industry-standard EDA tools for layout, simulation, and verification, and analyze real-world design challenges, preparing them for professional roles in VLSI design and verification.

3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

Introduction to Physical Design, VLSI Physical Design Flow

PC1: Demonstrated understanding of VLSI physical design concepts, including the physical design flow from RTL (Register Transfer Level) to GDSII (Graphic Data System II).

PC2: Ability to describe the industry-standard flow for VLSI physical design, encompassing fabrication processes such as CMOS technology and photolithography.

Verification Techniques

PC3: Proficiency in functional verification methodologies, utilizing simulation tools and testbenches to ensure design correctness and coverage analysis.

PC4: Competency in timing verification using Static Timing Analysis (STA) to identify and mitigate timing violations and uncertainties.

Design Tools and EDA

PC5: Practical knowledge of Electronic Design Automation (EDA) tools for layout editing, including place and route tools and the use of cell libraries.

PC6: Ability to use verification tools like Static Timing Analysis (STA) tools and Layout vs. Schematic (LVS) checkers to ensure design accuracy and compliance with specifications.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Gain a foundational understanding of VLSI physical design, encompassing the industry-standard flow from RTL to GDSII. Explore RTL design and synthesis techniques using Verilog/VHDL, along with strategies for placement, routing, clock tree synthesis, and optimization of power grids.

- Gain expertise in essential verification methodologies crucial for VLSI design, encompassing functional verification through simulation and comprehensive coverage analysis using test-benches.
- Acquire proficiency in Electronic Design Automation (EDA) tools used in VLSI design, covering layout editors, place and route tools, and cell libraries.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1. Proficiency in utilizing Electronic Design Automation (EDA) tools for layout editing, including place and route functionalities and management of cell libraries.

GS2. Competence in employing simulation tools such as Verilog/VHDL simulators and waveform viewers to validate functional correctness and performance metrics.

GS3. Ability to conduct various verification techniques, including Static Timing Analysis (STA) and Layout vs. Schematic (LVS) checking, to ensure design integrity and adherence to specifications.

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project Marks	Viva Marks
Fundamentals of VLSI Physical Design and Verification	**Introduction to Physical Design ,VLSI Physical Design Flow**	30	20	-	6
	● Demonstrated understanding of VLSI physical design concepts, including the physical design flow from RTL (Register Transfer Level) to GDSII (Graphic Data System II).	-	-	-	-
	● Ability to describe the industry-standard flow for VLSI physical design, encompassing fabrication processes such as CMOS technology and photolithography.	-	-	-	-
	Verification Techniques	30	20	-	7

	• Proficiency in functional verification methodologies, utilizing simulation tools and testbenches to ensure design correctness and coverage analysis.	-	-	-	-
	• Competency in timing verification using Static Timing Analysis (STA) to identify and mitigate timing violations and uncertainties.	-	-	-	-
	Design Tools and EDA	40	20	-	7
	• Practical knowledge of Electronic Design Automation (EDA) tools for layout editing, including place and route tools and the use of cell libraries.	-	-	-	-
	• Ability to use verification tools like Static Timing Analysis (STA) tools and Layout vs. Schematic (LVS) checkers to ensure design accuracy and compliance with specifications.	-	-	-	-
	Total Marks -200	**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.