QUALIFICATION FILE – Standalone NOS

Essentials of System Verilog and UVM based Verification

☐ Horizontal/Generic ☐ Vertical/Specialization

☒ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☒ OEM

NCrF/NSQF Level: 5

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

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<tr><td>2.</td><td>Sector/s</td><td colspan="2">Electronics</td></tr>
<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version (Will be issued after NSQC approval.)</td><td>NG-05-EH-02906-2024-V1-NIELIT</td><td>5. NCrF/NSQF Level: 5</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">The Standalone NOS encompasses Integrated Circuit (IC) and System on Chip (SoC) verification, starting with Verilog HDL for RTL verification, test benches, and test automation, then advancing to System Verilog, C/C++, and scripting languages like Linux shell scripting, Perl, and Python. It covers processor architecture, including ISA fundamentals, RISC-V, DIR-V Microprocessors, and bus architecture. SoC verification topics include DIR-V processor-based SoCs, AXI Bus architecture, and various verification methodologies like ABV, CDV, and UVM.

The syllabus concludes with SoC emulation, post-silicon validation, FPGA architectures, embedded C programming, and performance benchmarking.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
<table>
<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Relevant Experience (with Specialization - if applicable)</th></tr>
<tr><td>1</td><td>2nd year of UG in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches</td><td>NA</td></tr>
<tr><td>2</td><td>3 Years of Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 10th</td><td>1.5 Years</td></tr>
<tr><td>3</td><td>2 Year of diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 12th</td><td>NA</td></tr>
</table></td></tr>
</table>

4	NSQF Level 4.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years
5	NSQF Level 4 Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years

b. Age: 18 Years

8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	2 Credits	**9. Common Cost Norm Category (I/II/III)** *(wherever applicable)***:** Category- I
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA	
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☒ **Offline** ☐ **Online** ☐ **Blended**	

Training Delivery Mode	Theory (Hours)	Practical (Hours)	Total (Hours)
Classroom (offline)	30	30	60

The mode of delivery shall be based on the regional demand and can be offered in anyof the above modes mentioned.

12. Assessment Criteria

Theory (Marks)	Practical (Marks)	Project/ Presentation /Assignment (Marks)	Viva/ Internal Assessment (Marks)	Total (Marks)	Passing %age
100	60	20	20	200	50

The centralised online assessment is conducted by the Examination Wing, NIELIT Headquarters.

13.	**Is the NOS Amenable to Persons with Disability**	☒ **Yes** ☐ **No If "Yes", specify applicable type of Disability:** **a)** Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims **b)** Visual Impairment: Low Vision	
14.	**Progression Path After Attaining the Qualification, wherever applicable** *(Please show Professional and Academic progression)*	Design Engineer->Application Engineer->Team Lead -> Project Manager	
15.	**How participation of women will be encouraged?**	Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women's participation under other schemes launched by the Government from time to time.	
16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	Qualification files available in English & Hindi Language.	
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	Name: Jayaraj U Kidav Email: jayaraj@nielit.gov.in Website: https://nielit.gov.in/ Name: Ishant Kumar Bajpai Email: ishant@nielit.gov.in Website: https://nielit.gov.in/ Name: Deepam Dubey Email: deepamdubey@nielit.gov.in Website: https://nielit.gov.in/ Name: Sreejeesh S.G Email: sreejeesh@nielit.gov.in Website: https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI Design
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI Design
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No Available at Annexure-II
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B. Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech.

4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted
5.	**Tools and Equipment Required for Assessment**	Same as for training ☒ Yes ☐ No

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided: 7
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure:** Industry Validation	*Available at* Annexure-III: Industry Validation
4.	**Annexure:** Training Details	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning

6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	• Demonstrate a deep understanding of Verilog HDL and System Verilog for RTL design and functional verification. This includes creating test benches, automating verification processes, and analyzing assertions and coverage metrics. • Expertise in theoretical concepts and practical simulation techniques for verifying processor functionalities, ensuring robust processor performance and integration. • Proficient in designing, simulating, and verifying SoC systems while leveraging FPGA-based emulation and post-silicon validation processes to ensure system reliability and performance.	• These job role outcomes reflect a strong foundation in hardware description languages like Verilog and System Verilog, enabling professionals to design and verify RTL and functional models effectively. • Expertise in processor simulation and verification techniques ensures reliable processor integration and performance optimization. • Proficiency in SoC design, simulation, and FPGA-based emulation guarantees system reliability and thorough validation, aligning theoretical knowledge with industry standards.	5
Professional and Technical Skills/ Expertise/ Professional Knowledge	• Strong knowledge of verification processes, including test automation, assertions, and coverage analysis, with scripting skills in languages like	• The job role demands strong technical expertise in verification processes, leveraging test automation, assertions, and coverage	5

	Python, Perl, and Linux shell scripting. • Capability to design and verify SoC systems, utilizing AXI bus architecture, peripheral interfacing, and creating verification IPs using methodologies like UVM. • Ability to perform SoC emulation, write embedded C test programs, and carry out post-silicon validation, ensuring robust system performance and reliability.	analysis, combined with proficiency in scripting languages like Python, Perl, and Linux shell scripting. • It requires the capability to design and verify SoC systems using AXI bus architecture, peripheral interfacing, and UVM-based verification IPs. • Additionally, it emphasizes the ability to perform FPGA-based SoC emulation, write embedded C test programs, and execute post-silicon validation to ensure system reliability and optimal performance.	
Employment Readiness & Entrepreneurship **Skills & Mind-set/Professional Skill**	• Equips candidates to contribute effectively to verification and validation projects, ensuring ICs and SoCs meet performance and reliability. • Demonstrate the ability to build verification environments for complex SoCs, develop test automation frameworks, and perform FPGA-based emulation and post-silicon validation. • Empowers individuals to innovate and launch custom processor-based solutions, addressing niche markets and driving entrepreneurial ventures in the semiconductor domain.	• This outcome ensures that candidates are job-ready by imparting the technical skills required for comprehensive verification and validation of ICs and SoCs. • By fostering innovation in custom processor-based solutions, candidates are prepared to address market demands and identify niche opportunities.	5
Broad Learning Outcomes/Core Skill	• Demonstrate the ability to create and analyze test benches, automate verification processes, and use advanced verification techniques like assertions and coverage analysis. • Integrate AXI bus architecture, peripheral interfacing, and IP verification using methodologies like UVM to ensure robust system design. • Perform FPGA-based SoC emulation, write	• The above job role equips individuals with proficiency in functional verification and test automation, enabling them to create and analyze test benches, automate processes, and utilize scripting tools effectively. • It ensures competence in processor and SoC design and verification, with expertise in methodologies like UVM and AXI architecture.	5

	embedded C test programs, and implement post-silicon validation to ensure performance and reliability.	Additionally, it develops skills in SoC emulation and post-silicon validation, emphasizing reliability, performance, and adherence to industry standards.	
Responsibility	• Take responsibility for designing and executing verification environments, including test benches and automation, ensuring ICs, processors, and SoCs meet functionality and industry standards.	• The job role emphasizes taking ownership of the verification and validation processes to ensure ICs, processors, and SoCs meet functional and quality standards. • It involves responsibility for implementing advanced methodologies like UVM and ABV, ensuring the reliability and compliance of designs. Managing end-to-end verification, from simulation to post-silicon validation, reflects accountability for delivering error-free, optimized embedded systems.	5

Annexure-II: Tools and Equipment (lab set-up)

LIST OF EQUIPMENT (For a batch of 30 students)

	Description	Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	

6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
2	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
3	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
4	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba,	9434996748	bginfotech2007@gmail.com

				Medinipur		
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com
6	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com
7	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2024-25	500	200	20
2025-26	500	200	20
2026-27	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	☐Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80

2	☐Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
3	☐Showing Practical Demonstrations to the learners	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
4	☐Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
5	☐Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
6	☐Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	☐On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Design Software	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. Description:

This NOS covers comprehensive training in integrated circuit and processor verification, spanning Verilog HDL and System Verilog for RTL verification, advanced functional verification techniques, scripting languages for automation, processor architecture including RISC-V and DIR-V microprocessors, SoC verification methodologies, and FPGA-based emulation for SoC validation and performance evaluation.

2. Scope:

The scope covers the following:

The NOS covers Verilog HDL and System Verilog for integrated circuit verification, emphasizing RTL verification, test bench creation, and automation with scripting languages. It includes detailed exploration of processor architecture, encompassing RISC-V and DIR-V

microprocessors, focusing on simulation, verification planning, and functional coverage assessment. The module also delves into SoC verification methodologies, including AXI bus architecture, UVM-based verification environments, and FPGA emulation for post-silicon validation and performance evaluation.

3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

Integrated Circuit verification.

- Proficient in Verilog HDL for RTL verification, encompassing the creation of diverse test benches, formulation of comprehensive test cases, and implementation of streamlined verification architectures.
- Proficiency in System Verilog for advanced verification techniques, utilizing simulators, and effectively applying coverage metrics for comprehensive verification.
- Competence in scripting languages like Linux shell scripting, Perl, and Python for automation in verification processes.

Processor Architecture and Processor verification, SoC Verification

- Proficiency in processor architecture and verification, including understanding ISA concepts, memory hierarchy, and advanced architectures like superscalar processors, accelerators, and vector processors. Extensive knowledge of DIR-V microprocessors, focusing on microcontroller-class features, addressing schemes, memory mapping, and arbitration protocols.
- Expertise in system-on-chip (SoC) verification, particularly with DIR-V processor-based SoCs. In-depth understanding of SoC architectures, including peripheral components, memory structures, and basic building blocks. Mastery of verification methodologies such as assertion-based verification (ABV), coverage-driven verification (CDV), and constraint random verification (CRV). Skilled in developing verification IPs and environments.
- Practical proficiency in Universal Verification Methodology (UVM), enabling the construction of effective SoC verification environments. Experience in writing advanced test cases and executing verification projects involving DIR-V and Swadeshi processor-based SoCs.

Methodology based SoC Verification, SoC Emulation and post silicon Validation

- Proficient in Universal Verification Methodology (UVM), capable of constructing robust SoC verification environments.

- Skilled in writing complex test cases to ensure thorough verification of DIR-V and Swadeshi processor-based SoCs.
- Experienced in executing verification projects, applying UVM methodologies effectively to achieve reliable SoC validation.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Proficiency in Verilog HDL for RTL verification, encompassing test bench creation, test case development, verification architecture, automation, assertions, and coverage metrics.
- Expertise in processor architecture, including ISA fundamentals, memory hierarchy, DIR-V microprocessor features like address mapping and arbitration, and simulation for verification, with emphasis on functional coverage.
- Comprehensive understanding and practical application of SoC verification methodologies, including UVM-based environments, IP verification, test case automation, and validation using FPGA emulation for DIR-V processor-based designs.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

- Proficient in Verilog HDL and System Verilog, mastering RTL verification through test bench creation, test case development, and setting up verification architectures, alongside expertise in C and object-oriented programming essential.
- Proficient application of Universal Verification Methodology (UVM) to build robust SoC verification environments, incorporating assertion-based verification (ABV), coverage-driven verification (CDV), and constraint random verification (CRV) for comprehensive verification coverage.
- Comprehensive expertise in processor architecture, encompassing instruction set architecture (ISA), memory hierarchy, and advanced features like superscalar and vector processors, alongside specialized knowledge of DIR-V microprocessors, addressing mechanisms, bus architecture, and memory mapping crucial for robust processor simulation and verification.

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project Marks	Viva Marks
Essentials of System Verilog and UVM based Verification **NOS Code: NIE/ELE/N0118**	**Integrated Circuit verification.**	30	20	-	6
	● Proficient in Verilog HDL for RTL verification, encompassing the creation of diverse test benches, formulation of comprehensive test cases, and implementation of streamlined verification architectures.	-	-	-	-
	● Proficiency in System Verilog for advanced verification techniques, utilizing simulators, and effectively applying coverage metrics for comprehensive verification.	-	-	-	-
	● Competence in scripting languages like Linux shell scripting, Perl, and Python for automation in verification processes.	-	-	-	-
	Processor Architecture and Processor verification, SoC Verification	30	20	-	7
	● Proficiency in processor architecture and verification, including understanding ISA concepts, memory hierarchy, and advanced architectures like superscalar processors, accelerators, and vector processors. Extensive knowledge of DIR-V microprocessors, focusing on microcontroller-class features, addressing schemes, memory mapping, and arbitration protocols.	-	-	-	-
	● Expertise in system-on-chip (SoC) verification, particularly with DIR-V processor-based SoCs. In-depth understanding of SoC architectures, including peripheral components, memory structures, and basic building blocks. Mastery of verification methodologies such as assertion-based verification (ABV), coverage-driven verification (CDV), and constraint random verification (CRV). Skilled in developing verification IPs and environments.	-	-	-	-

	● Practical proficiency in Universal Verification Methodology (UVM), enabling the construction of effective SoC verification environments. Experience in writing advanced test cases and executing verification projects involving DIR-V and Swadeshi processor-based SoCs.	-	-	-	-
	Methodology based SoC Verification, SoC Emulation and post silicon Validation	**40**	**20**	**-**	**7**
	● Proficient in Universal Verification Methodology (UVM), capable of constructing robust SoC verification environments.	-	-	-	-
	● Skilled in writing complex test cases to ensure thorough verification of DIR-V and Swadeshi processor-based SoCs.	-	-	-	-
	● Experienced in executing verification projects, applying UVM methodologies effectively to achieve reliable SoC validation.	-	-	-	-
	Total Marks -200	**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.