QUALIFICATION FILE – Standalone NOS

Essentials of SoC Design for Verification

☐ Horizontal/Generic ☐ Vertical/Specialization

☒ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☒ OEM

NCrF/NSQF Level: 5

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

NIELIT Bhawan,
Plot No. 3, PSP Pocket, Sector-8,
Dwarka, New Delhi-110077,
Phone:- 91-11-2530 8300
e-mail:- contact@nielit.gov.in

Table of Contents

Section 1: Basic Details

1.	**NOS-Qualification Name**	**Essentials of SoC Design for Verification**	
2.	**Sector/s**	Electronics	
3.	**Type of Qualification ☒ New ☐ Revised**	**NQR Code & version of the existing /previous qualification:** NA	**Qualification Name of the existing/previous version:** NA
4.	**National Qualification Register (NQR) Code & Version** *(Will be issued after NSQC approval.)*	NG-05-EH-02912-2024-V1-NIELIT	**5. NCrF/NSQF Level: 5**
6.	**Brief Description of the Standalone NOS**	The SoC Design and Verification NOS provides advanced training in designing and verifying System-on-Chip (SoC) architectures. It covers multi-core SoCs, hardware accelerators, and peripheral interfacing. Students learn Universal Verification Methodology (UVM) for building test benches and verifying IPs and SoCs, focusing on the DIR-V processor. The module includes FPGA emulation for AMD and Xilinx architectures, with logic synthesis and timing considerations. Practical tasks include FPGA porting, software development, and Linux porting on DIR-V processor-based SoCs. It also explores high-level synthesis, AI/ML hardware accelerator design, and SoC performance evaluation. This prepares students for complex SoC verification and validation challenges in real-world scenarios.	
7.	**Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee**	**a. Entry Qualification & Relevant Experience:**	

S. No.	Academic/Skill Qualification (with Specialization - if applicable)	Relevant Experience (with Specialization - if applicable)
1	2nd year of UG in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	NA
2	3 Years of Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 10th	1.5 Years
3	2 Year of diploma in Electronics and	NA

			Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 12th	
		4	NSQF Level 4.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years
		5	NSQF Level 4 Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years

b. Age: 18 Years

8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	2 Credits	**9. Common Cost Norm Category (I/II/III)** *(wherever applicable)***:** Category-I
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA	
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☒ **Offline** ☐ **Online** ☐ **Blended**	

Training Delivery Mode	Theory (Hours)	Practical (Hours)	Total (Hours)
Classroom (offline)	30	30	60

The mode of delivery shall be based on the regional demand and can be offered in anyof the above modes mentioned.

12. Assessment Criteria

Theory (Marks)	Practical (Marks)	Project/ Presentation /Assignment (Marks)	Viva/ Internal Assessment (Marks)	Total (Marks)	Passing %age
100	60	20	20	200	50%

		The centralized online assessment is conducted by the Examination Wing, NIELIT Headquarters.	
13.	**Is the NOS Amenable to Persons with Disability**	☒ **Yes** ☐ **No** **a)** Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims **b)** Visual Impairment: Low Vision	
14.	**Progression Path After Attaining the Qualification, wherever applicable** *(Please show Professional and Academic progression)*	Design/Application Engineer/Team Lead/Project Manager	
15.	**How participation of women will be encouraged?**	Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women's participation under other schemes launched by the Government from time to time.	
16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	Qualification files available in English & Hindi Language	
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No** **URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	Name: Jayaraj U Kidav Email: jayaraj@nielit.gov.in Website: https://nielit.gov.in/ Name: Ishant Kumar Bajpai Email: ishant@nielit.gov.in Website: https://nielit.gov.in/ Name: Deepam Dubey Email: deepamdubey@nielit.gov.in Website: https://nielit.gov.in/ Name: Sreejeesh S.G Email: sreejeesh@nielit.gov.in Website: https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI Design
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI Design
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No *(If "Yes", details to be provided in Annexure)*
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B. Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.

3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech.
4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted
5.	**Tools and Equipment Required for Assessment**	Same as for training ☒ Yes ☐ No

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided: 7
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure:** Industry Validation	*Available at* Annexure-III: Industry Validation
4.	**Annexure:** Training Details	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning
6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	• Demonstrate a comprehensive understanding of Multi-Core SoCs, hardware accelerators, and their peripheral interfaces. • Understand the FPGA design flow, including logic synthesis, timing, and porting emulated SoCs onto hardware platforms like AMD/Xilinx FPGAs. • Gain theoretical knowledge of high-level synthesis and design techniques for AI/ML hardware accelerators.	• The job role/outcomes build a strong foundation in understanding SoC architectures, including Multi-Core SoCs, hardware accelerators, and their integration processes. • They emphasize theoretical expertise in FPGA design flow, post-silicon validation, and Universal Verification Methodology (UVM) for verifying and validating complex SoC environments.	5
Professional and Technical Skills/ Expertise/ Professional Knowledge	• Expertise in building UVM-based test benches, creating IP and SoC verification environments, writing test cases, and implementing automation frameworks for effective system validation. • Advanced skills in FPGA design flow, logic synthesis, and timing analysis using popular architectures like AMD/Xilinx. Ability to perform FPGA-based emulation, port SoC designs, and validate functionality through embedded C programming. • Comprehensive understanding of high-level synthesis and AI/ML hardware accelerator design, enabling efficient performance evaluation, benchmarking, and optimization of SoC systems in real-world applications.	• The job role emphasizes advanced expertise in SoC verification methodologies, requiring candidates to build UVM-based environments, automate testing, and validate IPs effectively. Proficiency in FPGA design and emulation ensures seamless integration, porting, and validation of SoCs using industry-standard tools and architectures.	5
Employment Readiness & Entrepreneurship	• Demonstrate expertise in developing UVM-based verification environments, automating test cases, and ensuring compliance with industry verification	• The job role equips individuals with advanced skills in SoC verification, emphasizing UVM-based test environments and automation,	5

Skills & Mind-set/Professional Skill	standards, making candidates job-ready for VLSI design and verification roles. • Showcase the ability to execute FPGA porting, embedded software development, and post-silicon validation, ensuring robust system performance and meeting industry demands.	aligning with industry demands for VLSI verification experts. It fosters expertise in FPGA-based emulation and post-silicon validation, ensuring candidates are well-prepared for high-performance embedded system roles.	
Broad Learning Outcomes/Core Skill	• Ability to design and debug complex SoC systems by leveraging UVM methodologies, building verification environments, and addressing functional and timing challenges in advanced multi-core architectures. • Competence in documenting and presenting verification plans, simulation results, and performance benchmarks, while effectively collaborating in multi-disciplinary teams for SoC design and validation projects. • Skill to integrate AI/ML hardware accelerators and apply FPGA-based emulation techniques, staying updated with the latest innovations in SoC design and verification methodologies.	• The job role/outcomes emphasize problem-solving and analytical thinking, enabling professionals to design, debug, and verify complex SoC systems using advanced methodologies like UVM. It requires strong technical communication skills to document verification plans and collaborate effectively with multi-disciplinary teams.	5
Responsibility	• Candidate must take responsibility for building robust verification environments to guarantee the functional correctness of complex SoCs, including IP-level and system-level verification. • Compliance and Validation: Demonstrate accountability for adhering to verification methodologies and standards while performing SoC emulation, post-silicon validation, and performance benchmarking to ensure reliability and compliance. • End-to-End Project Ownership: Take ownership of the entire SoC design verification and validation lifecycle, including planning, execution, debugging, and delivery of verified systems ready for production or deployment.	• The job role emphasizes taking responsibility for the integrity of verification processes, ensuring that SoC systems are thoroughly tested and meet performance requirements. Candidates must uphold standards of compliance and validation, ensuring accuracy during emulation and post-silicon stages.	5

Annexure-II: Tools and Equipment (lab set-up)

LIST OF EQUIPMENT

(For a batch of 30 students)

Description		Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
2	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
3	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
4	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba, Medinipur	9434996748	bginfotech2007@gmail.com
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com
6	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com
7	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2024-25	500	200	20
2025-26	500	200	20
2026-27	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	☐Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
2	☐Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
3	☐Showing Practical Demonstrations to the learners	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
4	☐Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80

5	☐Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
6	☐Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	☐On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Design Software	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. Description:

This Standalone NOS provides an in-depth understanding of advanced System-on-Chip (SoC) design and verification methodologies. It covers multi-core SoCs, hardware accelerators, and UVM-based SoC verification environments, including hands-on case studies like DIR-V processor verification. Additionally, the course explores SoC emulation, FPGA-based verification, post-silicon validation, and high-level synthesis for AI/ML hardware accelerators. Students will engage in real-world projects, including Linux porting, benchmarking, and performance evaluation, preparing them for modern SoC development and testing challenges.

2. Scope:

The scope covers the following:

- The scope of this course encompasses advanced SoC design, verification, and validation methodologies, focusing on multi-core SoCs, hardware accelerators, and Universal Verification Methodology (UVM). It also covers FPGA-based emulation, post-silicon validation, and high-level synthesis for AI/ML hardware. Students will gain hands-on experience in SoC testing, performance evaluation, Linux porting, and application development, preparing them for industry roles in modern SoC development and verification.

3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

Advanced SoCs and methodology based SoC Verification

- Gain comprehensive knowledge of Multi-Core SoCs, including their architectural nuances and effective integration strategies with hardware accelerators and peripheral interfaces.
- Utilize Universal Verification Methodology (UVM) components proficiently to construct robust test benches and verification environments tailored to SoC designs.
- Demonstrate proficiency in conducting IP verification using UVM through practical application in a specified case study scenario.
- Develop and deploy a comprehensive UVM-based SoC verification environment, emphasizing the creation and automation of test cases to ensure thorough verification coverage.

SoC Emulation and Post silicon verification and validation

- Gain expertise in the design flow of AMD/Xilinx FPGA architectures, focusing on effective emulation techniques for SoC applications.
- Apply advanced logic synthesis and timing concepts to optimize FPGA designs for System-on-Chip applications.
- Utilize embedded logic analyzers proficiently for debugging and verifying FPGA-based SoC designs, ensuring robust functionality.
- Demonstrate expertise in porting and emulating DIR-V processor-based SoCs on FPGA platforms, including the development and rigorous testing of embedded ‘C’ programs.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Gain in-depth knowledge of Multi-Core SoCs, encompassing their architectures and effective integration with hardware accelerators and peripheral interfaces.
- Gain mastery in UVM components and methodologies to construct robust test benches, perform IP verification, and create comprehensive SoC verification environments.
- Gain mastery in popular AMD/Xilinx FPGA architectures and their design flow to proficiently emulate SoCs. Apply advanced logic synthesis and timing concepts to optimize FPGA designs for diverse applications, ensuring effective emulation. Utilize embedded logic analyzers competently for thorough debugging and verification during FPGA emulation processes.
- Develop proficiency in porting and emulating DIR-V processor-based SoCs on FPGA platforms, including the creation and validation of embedded 'C' programs.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1. Gain expertise in Universal Verification Methodology (UVM) components for building robust test benches, conducting IP verification, and automating test cases in SoC environments.

GS2. Understand the architecture and integration of Multi-Core SoCs with hardware accelerators and peripheral interfaces.

GS3. Gain mastery in FPGA design flow, logic synthesis, and timing optimization tailored for SoC applications using popular AMD/Xilinx architectures. Develop expertise in porting and emulating DIR-V processor-based SoCs on FPGA platforms, encompassing embedded software development and Linux application execution.

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project Marks	Viva Marks
Essentials of SoC Design for Verification	**Advanced SoCs and methodology based SoC Verification**	50	30	-	10
	• Gain comprehensive knowledge of Multi-Core SoCs, including their architectural nuances and effective integration strategies with hardware accelerators and peripheral interfaces.	-	-	-	-
	• Utilize Universal Verification Methodology (UVM) components proficiently to construct robust test benches and verification environments tailored to SoC designs.	-	-	-	-
	• Demonstrate proficiency in conducting IP verification using UVM through practical application in a specified case study scenario.	-	-	-	-
	• Develop and deploy a comprehensive UVM-based SoC verification environment, emphasizing the creation and automation of test cases to ensure thorough verification coverage.	-	-	-	-
	SoC Emulation and Post silicon verification and validation	50	30	-	10
	• Gain expertise in the design flow of AMD/Xilinx FPGA architectures, focusing on effective emulation techniques for SoC applications.	-	-	-	-
	• Apply advanced logic synthesis and timing concepts to optimize FPGA designs for System-on-Chip applications.	-	-	-	-
	• Utilize embedded logic analyzers proficiently for debugging and verifying FPGA-based SoC designs, ensuring robust functionality.	-	-	-	-
	• Demonstrate expertise in porting and emulating DIR-V processor-	-	-	-	-

	based SoCs on FPGA platforms, including the development and rigorous testing of embedded 'C' programs.				
	Total Marks -200	**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.