QUALIFICATION FILE-Standalone NOS

Essentials of Semiconductors Assembly Test Marking and Packaging

☐ Horizontal/Generic ☐ Vertical/Specialization

☐ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☐ OEM

NCrF/NSQF Level: 4.5

Submitted By:

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Table of Contents

Section 1: Basic Details

<table>
<tr><td>1.</td><td>NOS-Qualification Name</td><td colspan="2">Essentials of Semiconductors Assembly Test Marking and Packaging</td></tr>
<tr><td>2.</td><td>Sector</td><td colspan="2">Electronics</td></tr>
<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version</td><td>NG-4.5-EH-03735-2025-V1-NIELIT</td><td>5. NCrF/NSQF Level: 4.5</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">This Standalone NOS provides an in-depth understanding of the fundamental concepts and practices involved in semiconductor assembly, test, marking, and packaging (ATMP), with a special emphasis on defect analysis and quality control. The course also addresses the entire process flow from fabricated wafer to final packaging, with a focus on the tools, techniques, and quality control measures critical to producing reliable semiconductor devices.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
<table>
<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Required Experience (with Specialization - if applicable)</th></tr>
<tr><td>1.</td><td>3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th</td><td>NA</td></tr>
<tr><td>2</td><td>3rd year of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th</td><td>NA</td></tr>
<tr><td>3</td><td>1st year of UG in Electronics Engineering/Physics/ allied fields</td><td>NA</td></tr>
<tr><td>4</td><td>12th Pass</td><td>1.5-year experience in ESDM Sector.</td></tr>
<tr><td>5</td><td>10th pass plus 2-year NTC in relevant field of Electronics Sector</td><td>1.5-year experience in ESDM Sector.</td></tr>
</table></td></tr>
<tr><td>8.</td><td>Credits Assigned to this NOS-Qualification, Subject to Assessment (as per National Credit Framework (NCrF))</td><td>6 Credits</td><td>9. Common Cost Norm Category (I/II/III) (wherever applicable): Category-I</td></tr>
<tr><td>10.</td><td>Any Licensing Requirements for Undertaking Training on</td><td colspan="2">NA</td></tr>
</table>

<table>
<tr><td></td><td>This Qualification (wherever applicable)</td><td></td></tr>
<tr><td>11.</td><td>Training Duration by Modes of Training Delivery (Specify Total Duration as per selected training delivery modes and as per requirement of the qualification)</td><td>☒Offline ☐Online ☐Blended
<table>
<tr><th>Training Delivery Modes</th><th>Theory (Hours)</th><th>Practical (Hours)</th><th>Project /Internship (Hours)</th><th>Total (Hours)</th></tr>
<tr><td>Classroom (offline)</td><td>36</td><td>84</td><td>60</td><td>180</td></tr>
</table></td></tr>
<tr><td>12.</td><td>Assessment Criteria</td><td>
<table>
<tr><th>Theory (Marks)</th><th>Practical (Marks)</th><th>Project (Marks)</th><th>Viva (Marks)</th><th>Total (Marks)</th><th>Passing %age</th></tr>
<tr><td>100</td><td>60</td><td>20</td><td>20</td><td>200</td><td>50</td></tr>
</table>
The centralized online assessment is conducted by the Examination Wing, NIELIT Headquarters.
*Assessment strategy shall be as per NIELIT Norms prevailing at times.</td></tr>
<tr><td>13.</td><td>Is the NOS Amenable to Persons with Disability</td><td>☒ Yes ☐ No
a. Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims
b. Visual Impairment: Low Vision</td></tr>
<tr><td>14.</td><td>Progression Path After Attaining the Qualification, wherever applicable</td><td>MEMS Backend Fabrication Engineer -> Semiconductor Fabrication Engineer</td></tr>
<tr><td>15.</td><td>How participation of women will be encouraged?</td><td>Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women’s participation under other schemes launched by the Government from time to time.</td></tr>
<tr><td>16.</td><td>Other Indian languages in which the Qualification & Model Curriculum are being submitted</td><td>Qualification file is available in English and Hindi languages.</td></tr>
<tr><td>17.</td><td>Is similar NOS available on NQR-if yes, justification for this qualification</td><td>☐ Yes ☒ No</td></tr>
<tr><td>18.</td><td>Name and Contact Details Submitting / Awarding Body SPOC
(In case of CS or MS, provide details of both Lead AB & Supporting ABs)</td><td>Name: Sh. Saurabh Kesari
Email: saurabhk@nielit.gov.in
Contact No.: 0240-2982021
Website: https://www.nielit.gov.in

Name: Sh. Shashank Kumar Singh</td></tr>
</table>

		Email: shashank@nielit.gov.in **Contact No.:** 0240-2982021 **Website:** https://www.nielit.gov.in **Name:** Sh. Ravi Ranjan Kumar **Email:** raviranjan@nielit.gov.in **Contact No.:** 0240-2982021 **Website:** https://www.nielit.gov.in	
19.	**Final Approval Date by NSQC:18.02.2025**	**20. Validity Duration: 3 Years**	**21. Next Review Date: 18.02.2028**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 2 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design. Or M.Sc. in Physics/Electronics/Material Science and allied branches; with 2 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design.
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design. Or M.Sc. in Physics/Electronics/Material Science and allied branches; with 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design.
3.	**Tools and Equipment Required for Training**	☒Yes ☐No Available at Annexure-II
4.	**In Case of Revised Qualification, Details of Any Upskilling Required for Trainer**	NA

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design. Or M.Sc. in Physics/Electronics/Material Science and allied branches 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design.
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online, and the paper comprise of MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I- card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech.
4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted
5.	**Tools and Equipment Required for Assessment**	Same as for training ☒ Yes ☐ No

Section 4: Evidence of the Need for the Standalone NOS

1.	Government /Industry initiatives/ requirement (Yes/No): Yes
2.	Number of Industry validation provided: The course has been developed in collaboration with TATA Electronics to support the development of skilled manpower for the upcoming semiconductor industry.
3.	Estimated number of people to be trained: 500
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF level/NSQF descriptors *(Mandatory)*	Available at Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for qualification *(Mandatory, except in case of online course)*	Available at Annexure-II: Tools and Equipment
3.	**Annexure:** Industry Validation	Available at Annexure-III: Industry Validation
4.	**Annexure:** Training Details	Available at Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case selected Mode of delivery is "Blended Learning")*	Available at Annexure-V: Blended Learning
6.	**Annexure/Supporting Document:** Standalone NOS- Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Detailed Assessment Criteria *(Mandatory)*	Available at Annexure-VII: Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	Available at Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	Available at Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum *(Mandatory – Public view)*	Available at Annexure-A: Model Curriculum

Annexure I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	● In-depth understanding of semiconductor assembly processes, testing methods, and packaging techniques.	● Relates to the descriptor by providing the theoretical foundation necessary for professionals to understand and apply assembly, testing, marking, and packaging processes.	4.5

Professional and Technical Skills/ Expertise/ Professional Knowledge	● Ability to operate and troubleshoot testing and marking machines. ● Proficiency in designing efficient packaging solutions and quality control methods.	● Relates by equipping learners with hands-on technical skills to apply their knowledge in real-world assembly, test, marking, and packaging scenarios, ensuring quality output.	4.5
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	● Prepared for roles such as Test Engineer, Packaging Engineer, or Assembly Technician. ● Ability to work in teams and manage production workflows.	● Aligns by ensuring learners are ready for employment in semiconductor assembly and testing, with an entrepreneurial mindset to improve processes and contribute to innovation.	4.5
Broad Learning Outcomes/Core Skill and Responsibility	● Take responsibility for ensuring product quality through testing, proper marking, and effective packaging. ● Ability to monitor assembly processes and ensure efficiency and compliance.	● Prepares learners to take responsibility for critical aspects of the semiconductor manufacturing process, ensuring quality and efficiency.	4.5

Annexure II: Tools and Equipment (Lab Set-Up)

Sl. No	Description	Qty.	Specifications
1	Classroom	1	30 Sq. m
2	Student Chair	30	-
3	Student Table	30	-
4	LCD Projector	1	-
5	Trainer Chair & Table	1	-
6	Pin up Board	1	-
7	White Board	1	-
8	Desktop Computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB
9	Desk jet printer	1	A4

List of Tools and Equipment

Packaging Equipment

- Wafer Dicing Machines (Mechanical and Laser)

- Die Attach Equipment (Epoxy, Eutectic, and Solder Bonding)
- Wire Bonding Machines (Ball and Wedge Bonding)
- Encapsulation and Moulding Machines (Transfer and Compression Moulding)
- Singulation Equipment (Sawing and Laser Cutting)

Inspection and Defect Analysis Tools

- Optical Microscopes
- Scanning Electron Microscopes (SEM)
- X-ray Inspection Systems
- Thermal Imaging Systems

Testing and Reliability Equipment

- Burn-In Test Chambers
- Electrical Test Systems (Parametric and Functional Testers)
- Statistical Process Control (SPC) Software

Advanced Packaging Equipment

- Equipment for 3D Packaging and TSV Integration
- Fan-Out Wafer-Level Packaging (FOWLP) Tools

Consumables

- Silicon Wafers
- Encapsulation Materials (Epoxy, Polymer)
- Die Attach Materials (Epoxy, Solder)
- Wire Bonding Wires (Gold, Aluminum)
- Cleaning Solvents (Isopropyl Alcohol, Acetone)

Safety and General Equipment

- Personal Protective Equipment (PPE: Gloves, Goggles, Lab Coats)
- Chemical Fume Hoods
- Emergency Spill Kits and Eye Wash Stations

General Tools

- Desktop Computers with Process Simulation Software
- Projectors and Whiteboards for Presentations

Annexure III: Industry Validations Summary

The course has been developed in collaboration with TATA Electronics to support the development of skilled manpower for the upcoming semiconductor industry.

Annexure IV: Training & Employment Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2025-26	**100**	**50**	**10**
2026-27	**200**	**70**	**15**
2027-28	**200**	**70**	**15**

Data to be provided year-wise for next 3 years.

Annexure V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools: NA

Annexure VI: Standalone NOS - Performance Criteria details

1. **Description:**

   This Course focuses on the critical processes involved in preparing semiconductor devices for use. It covers assembly techniques, functional and reliability testing, precision marking, and packaging to ensure product quality and performance. The course equips learners with the skills to manage the entire lifecycle of semiconductor device preparation for mass production.

2. **Scope:**

   - Understand the processes of component placement, soldering, and die bonding in semiconductor packaging.
   - Learn methods for testing functionality, reliability, and performance of semiconductor devices.
   - Explore precision marking, labeling, and packaging techniques to ensure the safety and traceability of semiconductor devices.

3. **Elements and Performance Criteria**
   To be competent, the user/individual on the job must be able to:

Elements	Performance Criteria
Introduction to Semiconductor Packaging and Defect Analysis	PC`1: Demonstrate the ability to identify and classify common packaging defects such as delamination, voids, and soldering issues through visual inspection and analysis. PC2: Apply defect analysis techniques to determine the root causes of packaging issues and recommend

	corrective actions to ensure high-quality semiconductor packaging.
Wafer Preparation, Dicing, and Defect Prevention	PC3: Demonstrate the ability to identify and classify common packaging defects such as delamination, voids, and soldering issues through visual inspection and analysis. PC4: Apply defect analysis techniques to determine the root causes of packaging issues and recommend corrective actions to ensure high-quality semiconductor packaging
Die Attach and Wire Bonding with Defect Mitigation	PC5: Perform die attach and wire bonding processes accurately, ensuring proper alignment, secure connections, and minimal defects in the semiconductor packaging. PC6: Implement defect mitigation strategies during die attach and wire bonding to minimize common issues such as poor adhesion, wire loop instability, and electrical failures
Encapsulation, Moulding and Defect Analysis	PC7: Execute encapsulation and moulding processes accurately to ensure proper sealing and protection of semiconductor devices, minimizing contamination and mechanical stress. PC8: Conduct defect analysis during encapsulation and moulding to identify issues like voids, cracks, or improper curing, and implement corrective actions to maintain product quality.
Package Marking, Singulation and Defect Inspection	PC9: Carry out package marking and singulation processes efficiently, ensuring precise labeling, separation, and preparation for shipment without damaging the semiconductor packages. PC10: Perform defect inspection on marked and singulated packages, identifying issues such as misprints, alignment errors, or package damage, and applying corrective measures to ensure quality standards are met.
Final Testing, Burn-In, Quality Assurance, and Defect Control	PC11: Conduct final testing and burn-in procedures to validate the functionality and reliability of semiconductor devices, ensuring they meet performance specifications under stress conditions. PC12: Implement quality assurance and defect control measures during the final testing phase to identify and address any potential defects, ensuring the delivery of high-quality, reliable semiconductor products.
Advanced Packaging Technologies and Defect Challenges	PC13: Apply advanced packaging technologies such as 3D stacking, flip-chip, and system-in-package (SiP) to enhance performance and functionality while minimizing defects in semiconductor devices. PC14: Identify and resolve defect challenges specific to advanced packaging, such as thermal management, electrical performance issues, and interconnect reliability, ensuring high-quality and durable packaging solutions.
Project/Internship	PC15: Students will undertake individual or group projects focused on semiconductor packaging and testing, emphasizing defect analysis and mitigation. PC16: The project will cover the full ATMP process with key deliverables including process design documentation, practical execution with testing, and a final report with presentation.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

KU1: Understand key processes like die bonding, wire bonding, and encapsulation, and their impact on product reliability.
KU2: Learn testing techniques (functional, parametric, reliability) to ensure semiconductor performance and quality.
KU3: Gain knowledge of marking, SMT, and packaging types for optimal electrical performance and thermal management.

5. Generic Skills (GS):

The user/individual on the job needs to know how to:

GS1: Develop the ability to identify potential manufacturability issues in semiconductor designs and apply critical thinking to find effective solutions, optimizing designs for higher yield and cost efficiency.
GS2: Improve their skills in effectively communicating technical information, collaborating with cross-functional teams (e.g., design, manufacturing, and testing), and presenting findings or design optimizations clearly.
GS3: Enhance attention to detail, ensuring that every aspect of the semiconductor design process from layout to material selection is carefully considered for manufacturability, quality, and process compatibility.

Annexure VII: Assessment Criteria

Detailed assessment criteria for each NOS/Module are as follows:

NOS/Module	Assessment Criteria for Performance Criteria/Learning Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
Introduction to Semiconductor Packaging and Defect Analysis	PC`1: Demonstrate the ability to identify and classify common packaging defects such as delamination, voids, and soldering issues through visual inspection and analysis. PC2: Apply defect analysis techniques to determine the root causes of packaging issues and recommend corrective actions to ensure high-quality semiconductor packaging.	12	8	-	-
Wafer Preparation, Dicing, and Defect	PC3: Demonstrate the ability to identify and classify common packaging defects such as delamination, voids, and soldering issues through visual inspection and analysis.	16	9	-	-

Prevention	PC4: Apply defect analysis techniques to determine the root causes of packaging issues and recommend corrective actions to ensure high-quality semiconductor packaging				
Die Attach and Wire Bonding with Defect Mitigation	PC5: Perform die attach and wire bonding processes accurately, ensuring proper alignment, secure connections, and minimal defects in the semiconductor packaging. PC6: Implement defect mitigation strategies during die attach and wire bonding to minimize common issues such as poor adhesion, wire loop instability, and electrical failures	16	8	-	-
Encapsulation, Moulding and Defect Analysis	PC7: Execute encapsulation and moulding processes accurately to ensure proper sealing and protection of semiconductor devices, minimizing contamination and mechanical stress. PC8: Conduct defect analysis during encapsulation and moulding to identify issues like voids, cracks, or improper curing, and implement corrective actions to maintain product quality.	16	9	-	-
Package Marking, Singulation and Defect Inspection	PC9: Carry out package marking and singulation processes efficiently, ensuring precise labeling, separation, and preparation for shipment without damaging the semiconductor packages. PC10: Perform defect inspection on marked and singulated packages, identifying issues such as misprints, alignment errors, or package damage, and applying corrective measures to ensure quality standards are met.	12	8	-	-
Final Testing, Burn-In, Quality Assurance, and Defect Control	PC11: Conduct final testing and burn-in procedures to validate the functionality and reliability of semiconductor devices, ensuring they meet performance specifications under stress conditions. PC12: Implement quality assurance and defect control measures during the final testing phase to identify and address any potential defects, ensuring the delivery of high-quality, reliable semiconductor products.	14	9	-	-
Advanced Packaging Technologies and Defect Challenges	PC13: Apply advanced packaging technologies such as 3D stacking, flip-chip, and system-in-package (SiP) to enhance performance and functionality while minimizing defects in semiconductor devices. PC14: Identify and resolve defect challenges specific to advanced packaging, such as thermal management, electrical performance issues, and interconnect reliability, ensuring high-quality and durable packaging solutions.	14	9	-	-
Project/Internship	PC15: Students will undertake individual or group projects focused on semiconductor packaging and testing, emphasizing defect analysis and mitigation. PC16: The project will cover the full ATMP process with key deliverables including process design documentation, practical execution with testing, and a final report with presentation.	-	-	20	-
Viva	Including all Elements	-	-	-	20
Grand Total		**100**	**60**	**20**	**20**

Annexure VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.
Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.
The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.
2. The assessor assigns roll number.
3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ
4. Pass percentage would be 50% marks.
5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.