QUALIFICATION FILE–Standalone NOS

Essentials of Semiconductor Fabrication Technology

☐ Horizontal/Generic ☐Vertical/Specialization

☐ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☐ OEM

NCrF/NSQF Level: 4

Submitted By:

National Institute of Electronics and Information Technology (NIELIT)
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Section 1: Basic Details

<table>
<tr><td>1.</td><td>NOS-Qualification Name</td><td colspan="2">Essentials of Semiconductor Fabrication Technology</td></tr>
<tr><td>2.</td><td>Sector/s</td><td colspan="2">Electronics</td></tr>
<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version</td><td>NG-04-EH-03726-2025-V1-NIELIT</td><td>5. NCrF/NSQF Level: 4</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">Implementing the NOS will significantly benefit the semiconductor industry by standardizing skills and knowledge, leading to higher quality and consistency. By aligning training with industry needs, it will enhance employability for individuals seeking careers in this field. Moreover, a skilled and competent workforce fostered by the NOS will contribute to increased productivity and efficiency, ultimately driving innovation and supporting the growth of the semiconductor industry.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
<table>
<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Relevant Experience (with Specialization - if applicable)</th></tr>
<tr><td>1</td><td>2 Years of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th</td><td>NA</td></tr>
<tr><td>2</td><td>12th Pass</td><td>NA</td></tr>
<tr><td>3</td><td>10th pass plus 2-year NTC in Electronics Sector</td><td>NA</td></tr>
</table></td></tr>
<tr><td>8.</td><td>Credits Assigned to this NOS-Qualification, Subject to Assessment (as per National Credit Framework (NCrF))</td><td>4 Credits</td><td>9. Common Cost Norm Category (I/II/III) (wherever applicable): Category-I</td></tr>
<tr><td>10.</td><td>Any Licensing Requirements for Undertaking Training on This Qualification (wherever applicable)</td><td colspan="2">NA</td></tr>
</table>

<table>
<tr><td>11.</td><td>Training Duration by Modes of Training Delivery (Specify Total Duration as per selected training delivery modes and as per requirement of the qualification)</td><td>☒Offline ☐ Online ☐ Blended
<table>
<tr><th>Training Delivery Mode</th><th>Theory (Hours)</th><th>Practical (Hours)</th><th>Total (Hours)</th></tr>
<tr><td>Classroom (offline)</td><td>26</td><td>94</td><td>120</td></tr>
</table></td></tr>
<tr><td>12.</td><td>Assessment Criteria</td><td>
<table>
<tr><th>Theory (Marks)</th><th>Practical (Marks)</th><th>Project/ Presentation /Assignment (Marks)</th><th>Viva/ Internal Assessment (Marks)</th><th>Total (Marks)</th><th>Passing %age</th></tr>
<tr><td>100</td><td>60</td><td>20</td><td>20</td><td>200</td><td>50</td></tr>
</table>
The centralized online assessment is conducted by the Examination Wing, NIELIT Headquarters.
*Assessment strategy shall be as per NIELIT Norms prevailing at times.</td></tr>
<tr><td>13.</td><td>Is the NOS Amenable to Persons with Disability</td><td>☒ Yes ☐ No
a. Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims
b. Visual Impairment: Low Vision</td></tr>
<tr><td>14.</td><td>Progression Path After Attaining the Qualification, wherever applicable</td><td>MEMS Backend Fabrication Engineer -> Semiconductor Fabrication Engineer</td></tr>
<tr><td>15.</td><td>How will the participation of women be encouraged?</td><td>Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women’s participation under other schemes launched by the Government from time to time.</td></tr>
<tr><td>16.</td><td>Other Indian languages in which the Qualification & Model Curriculum are being submitted</td><td>Qualification files available in English & Hindi Language.</td></tr>
<tr><td>17.</td><td>Is similar NOS available on NQR-if yes, justification for this qualification</td><td>☐Yes ☒ No</td></tr>
<tr><td>18.</td><td>Name and Contact Details Submitting / Awarding Body SPOC
(In the case of CS or MS, provide details of both Lead AB & Supporting ABs)</td><td>Name: Sh. Nandakumar.R
Email: nanda@nielit.gov.in/
Contact No.: 9995427802
Website: https://www.nielit.gov.in</td></tr>
</table>

		Name: **Sh. Sreejeesh SG** Email: sreejeesh@nielit.gov.in/ Contact No.: 9447769756 Website: https://www.nielit.gov.in	
19.	**Final Approval Date by NSQC: 18.02.2025**	**20. Validity Duration: 3 years**	**21. Next Review Date: 18.02.2028**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years) (as per NCVET guidelines)**	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches; with 2 years of relevant experience. Or M.Sc. in Physics/Electronics/Material Science and allied branches; with 2 years of relevant experience.
2.	**Master Trainer's Qualification and experience in the relevant sector (in years) (as per NCVET guidelines)**	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 3 years of relevant experience. Or M.Sc. in Physics/Electronics/Material Science and allied branches with 3 years of relevant experience.
3.	**Tools and Equipment Required for the Training**	☒ Yes ☐No Available at Annexure-II
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	Not Applicable

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 3 years of relevant experience. Or M.Sc. in Physics/Electronics/Material Science and allied branches with 3 years of relevant experience.
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech
4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted
5.	**Tools and Equipment Required for Assessment**	Same as for training ☒ Yes ☐ No

Section 4: Evidence of the Need for the Standalone NOS

1.	Government /Industry initiatives/ requirement (Yes/No): Yes
2.	Number of Industry validations provided: The course has been developed in collaboration with TATA Electronics to support the development of skilled manpower for the upcoming semiconductor industry.
3.	Estimated number of people to be trained: 500
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name.

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure:** Industry Validation	*Available at* Annexure-III: Industry Validation
4.	**Annexure:** Training Details	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning
6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-A: Model Curriculum

Annexure-I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	• **Understand and explain** the fundamental principles of semiconductor physics, including band theory, carrier transport mechanisms, and the behavior of p-n junctions. • **Analyze** the impact of different processing steps (e.g., photolithography, etching, doping) on the electrical and physical properties of semiconductor devices. • **Compare and contrast** various thin film deposition techniques (PVD, CVD) and their applications in semiconductor device fabrication.	The foundational knowledge gained in the course, such as understanding basic semiconductor physics and cleanroom procedures, aligns with the entry-level skills and knowledge expected at this level.	4

	• **Explain** the principles of cleanroom technology and the importance of maintaining a controlled environment for semiconductor manufacturing.		
Professional and Technical Skills/ Expertise/ Professional Knowledge	• Semiconductor Physics: Understanding of semiconductor principles, band theory, carrier transport mechanisms, and device physics. • Materials Science: Knowledge of semiconductor materials, their properties, and crystal structures. • Cleanroom Technology: Understanding of cleanroom principles, safety protocols, and contamination control measures.	• Possesses specialized professional and technical skills; displays clarity of professional knowledge and technical skills in a broad range of activities/ tasks. • Industry Standards: Familiarity with industry standards and best practices for semiconductor manufacturing.	4
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	• Strong Problem-solving & Critical Thinking: Developed through troubleshooting, data analysis, and identifying root causes of defects. • Enhanced Teamwork & Collaboration: Fostered through group projects and collaborative laboratory work.	• Developed Work Ethic & Professionalism: Emphasized by the cleanroom environment, demanding discipline, attention to detail, and safety adherence. • Cultivated a Continuous Learning Mindset: Encouraged by the dynamic nature of the semiconductor industry, emphasizing the need for ongoing learning and adaptation.	4
Broad Learning Outcomes/ Core Skill	• Demonstrate a comprehensive understanding of semiconductor physics, materials science, and cleanroom procedures. • Perform key semiconductor fabrication processes with accuracy and precision, including photolithography, thin film deposition, etching, and doping.	Apply critical thinking and problem-solving skills to troubleshoot process issues, analyze data, and optimize fabrication processes.	4
Responsibility	• Performing basic fabrication processes: This includes tasks such as photolithography, thin film deposition, etching, and doping, under supervision or independently. • Operating and maintaining fabrication equipment: This involves ensuring the proper functioning of equipment like spin coaters, etching systems, and deposition systems, as well as performing basic maintenance and troubleshooting. • Conducting basic metrology measurements: This includes using tools like ellipsometers and profilometers to measure film thicknesses, analyze surface roughness, and assess process variations.	Takes complete responsibility for maintaining a cleanroom environment: This includes adhering to cleanroom protocols, ensuring proper gowning procedures, and maintaining cleanliness and order within the work area.	4

	● Assisting with process development: This may involve participating in experiments, collecting and analyzing data, and assisting in the optimization of existing processes.		

Annexure II: Tools and Equipment (lab set-up)

Sl. No	Description	Qty.	Specifications
1	Classroom	1	30 Sq. m
2	Student Chair	30	-
3	Student Table	30	-
4	LCD Projector	1	-
5	Trainer Chair & Table	1	-
6	Pin up Board	1	-
7	White Board	1	-
8	Desktop Computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB
9	Desk jet printer	1	A4

List of Tools and Equipment:

Cleanroom Environment
- Cleanroom Facility
- Cleanroom Apparel (gowns, gloves, masks, shoe covers, hairnets)
- Cleanroom Consumables (wipes, tweezers, wafer handling tools)

Photolithography Tools
- Spin Coater
- Exposure Unit (UV Lithography System)
- Developer Station
- Hot Plates (Soft Bake and Hard Bake Stations)

Deposition Systems
- Physical Vapor Deposition (PVD) Tools (sputtering, thermal evaporation systems)
- Chemical Vapor Deposition (CVD) Systems (LPCVD, PECVD, ALD)

Etching Systems
- Wet Benches
- Reactive Ion Etching (RIE) System
- Inductively Coupled Plasma (ICP) Etching System

Doping and Oxidation Systems
- Ion Implanter
- Diffusion Furnace
- Rapid Thermal Annealing (RTA) System
- Thermal Oxidation Furnace

Metallization Tools
- Metal Deposition Systems
- Wire Bonders
- Patterning Tools

Metrology Tools
- Ellipsometer
- Profilometer
- Scanning Electron Microscope (SEM)
- Four-Point Probe
- Optical Microscope

Chemical Mechanical Planarization (CMP) Tools
- CMP Systems
- Slurry and Pads

Packaging Equipment
- Wire Bonding Machines
- Flip-Chip Bonders
- Testing Equipment

Software Tools
- Process Simulation Software (e.g., Silvaco, Synopsys)
- Data Analysis Software (e.g., MATLAB, Python)
- IC Design Software (e.g., Cadence Virtuoso)

General Laboratory Equipment
- Desktop Computers with Accessories
- Printers
- LCD Projector and Whiteboard

Consumables
- Silicon Wafers
- Photoresists
- Chemicals (etchants, solvents, cleaning agents)
- Process Gases (e.g., nitrogen, argon)

Optional Advanced Tools
- Atomic Force Microscope (AFM)
- Transmission Electron Microscope (TEM)

Annexure III: Industry Validations Summary

The course has been developed in collaboration with TATA Electronics to support the development of skilled manpower for the upcoming semiconductor industry.

Annexure IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2025-26	**100**	**50**	**10**
2026-27	**200**	**70**	**15**
2027-28	**200**	**70**	**15**

Data to be provided year-wise for the next 3 years.

Annexure V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools: NA

Annexure VI: Standalone NOS- Performance Criteria details

1. Description

This course provides a comprehensive introduction to semiconductor fabrication, covering key processes like wafer preparation, photolithography, etching, doping, and packaging. Through hands-on demonstrations and projects, learners gain practical skills in advanced manufacturing techniques and process optimization essential for careers in semiconductor and electronics industries.

2. Scope

The scope covers the following:

- Providing hands-on training in semiconductor fabrication, assembly, and testing processes to build practical skills.
- Delivering in-depth knowledge of core and advanced technologies used in modern semiconductor manufacturing.
- Preparing participants for diverse roles in the semiconductor industry, from process engineering to quality assurance and packaging.

3. Elements and Performance Criteria

Elements	Performance Criteria
Introduction to Semiconductor Fabrication	**PC1.** student can explain the fundamental concepts of semiconductor physics, including energy bands and charge carriers. **PC2.** Student can compare the electrical, optical, and thermal properties of silicon and III-V compounds. **PC3**. Student can describe the importance of a cleanroom in semiconductor manufacturing and Identify different cleanroom classifications and contamination control measures.
Wafer Manufacturing and Preparation	**PC4**. Student can describe the wafer slicing process, including the use of diamond wire saws and its impact on wafer thickness and material loss **PC5**. Student can explain Techniques and Applications of Epitaxial Growth **PC6**. Student can explain the principles and processes of the Czochralski and Float-Zone methods for crystal growth and Demonstrate understanding of factors affecting crystal quality, such as temperature control, rotation speed, and impurity levels.
Photolithography and Patterning	**PC7**. Theory: Fundamentals of Photolithography: Light Sources, Masks, and Photoresists. Process Steps: Spin Coating, Exposure, Development, and Hard Bake. Advanced Lithography Techniques and Applications **PC8**. Practical: Hands-on Lithography Process: Spin Coating to Development . Mask Alignment and Pattern Transfer Exercises
Etching Techniques	**PC9**. Theory: Introduction to Etching: Wet etching -Isotropic vs. Anisotropic Etching and Selectivity Control . Plasma-Based Dry Etching: Reactive Ion Etching (RIE), Inductively Coupled Plasma (ICP). Advanced Etching Techniques: Deep Reactive Ion Etching (DRIE) : -Wet vs. Dry Etching **PC10**. Practical : Demonstration: Wet and Dry Etching ; Demonstration: Etch Profile Analysis and Process Optimization
Thin Film Deposition Techniques	**PC11**. Theory: Overview of Deposition Techniques: Physical Vapor Deposition (PVD), Chemical Vapor Deposition (CVD); Techniques in PVD: Sputtering, Evaporation, E-beam. Techniques in CVD: LPCVD, PECVD, ALD ; Applications of Thin Films in Semiconductor Devices **PC12**. Practical: Demonstration: Thin Film Deposition Using PVD and CVD ; Demonstration: Measuring Film Thickness and Uniformity

Doping and Diffusion Processes	**PC13**. Theory : Fundamentals of Doping: Ion Implantation and Diffusion ; Dopant Profiles and Activation Techniques ; High-Temperature Annealing Processes and Rapid Thermal Annealing (RTA) ; Applications of Doping in Device Fabrication: p-n Junctions, Transistors **PC14**. Practical : Demonstration: Ion Implantation and Annealing Processes ;Demonstration: Doping Profile Characterization
Oxidation Processes	**PC15**. Theory : Thermal Oxidation of Silicon: Process and Kinetics ;Types of Oxidation: Dry vs. Wet Oxidation ;Rapid Thermal Oxidation (RTO) and its Applications ;Characterization of Oxide Layers: Thickness, Refractive Index, Dielectric Strength **PC16**. Practical: Demonstration: Oxidation Process; Demonstration: Oxide Thickness Measurement and Characterization
Metallization and Interconnect Formation	**PC17**. Theory: Fundamentals of Metallization: Metal Deposition, Patterning, and Etching; Materials for Interconnects: Aluminum, Copper, Tungsten; Techniques for Interconnect Formation: Damascene Process (single only), Electroplating; Challenges in Metallization: Electromigration, Resistance-Capacitance (RC) Delay **PC18**. Practical: Demonstration: Metallization and Interconnect Formation; Demonstration: Conductivity and Contact Resistance Measurements
Chemical Mechanical Planarization (CMP)	**PC19**. Theory : Principles of CMP: Material Removal, Planarization, and Surface Smoothing ; CMP Slurries and Pads: Composition and Selection Criteria ; Applications of CMP in Semiconductor Fabrication: Interlayer Dielectrics, Metal Layers; Challenges in CMP: Dishing, Erosion, Defectivity **PC20**. Practical Demonstration: CMP Process ;Demonstration: Surface Planarity and Roughness Measurement
Advanced Semiconductor Fabrication Techniques	**PC21**. Theory : Introduction to Advanced Techniques: MEMS Fabrication, 3D ICs, and More-than-Moore Technologies ; o Emerging Materials in Semiconductor Fabrication: SiC, GaN, Graphene ; Integration of Advanced Techniques in Modern Fabs ;Case Studies: Innovations in Semiconductor Manufacturing **PC22**: Practical : Demonstration: Advanced Fabrication Techniques ; Demonstration: Process Integration for Advanced Devices
Packaging and Assembly	**PC23**. :Theory :Overview of Semiconductor Packaging: Types, Materials, and Processes ; Techniques for Wire Bonding, Flip-Chip, and Wafer-Level Packaging ; Thermal and Mechanical Considerations in Packaging ; Testing and Reliability in Semiconductor Packaging **PC24**.:Practical Demonstration: Packaging Process ; Demonstration: Bonding Strength and Package Reliability Testing
Process Integration and Yield Management	**PC25**.:Theory : Integration of Fabrication Processes: Process Flow Design and Optimization ; Yield Management and Defect Reduction Techniques ; Statistical Process Control (SPC) and Process Monitoring ; Future Trends in Semiconductor Fabrication: Advanced Nodes, 3D Integration **PC26**. Practical :Demonstration: Process Integration Case Study ; Demonstration: Yield Analysis and Process Optimization

Reliability Testing and Failure Analysis	**PC27**. Theory : Fundamentals of Reliability Testing: Stress Testing, Burn-In, and Lifetime Testing ; Techniques for Failure Analysis: Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), X-ray Inspection ; Common Failure Mechanisms in Semiconductor Devices ; Strategies for Enhancing Reliability in Semiconductor Manufacturing **PC28**.Practical : Demonstration: Reliability Testing and Failure Analysis ; Demonstration: Conducting Stress Tests and Analyzing Device Failures
Final Project and Process Optimization	**PC29**. Practical: Final Project: Design and Implementation of a Semiconductor Fabrication Process ; Project Presentation and Evaluation

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

KU1: Understand semiconductor materials, crystal structures, and the importance of cleanroom environments and safety standards.

KU2. Learn crystal growth, wafer processing (slicing, polishing, cleaning), epitaxial growth, and defect management

KU3. Gain theoretical and practical knowledge in photolithography, etching, thin film deposition, doping, and oxidation

KU4. Explore advanced fabrication methods, emerging materials, and integration of processes into a full semiconductor manufacturing flow

KU5. Apply tools for yield optimization, statistical control, failure analysis, and ensure device reliability throughout the process

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1: Ability to identify process deviations, analyze data (e.g., defect density, yield loss), and apply root cause analysis to resolve fabrication issues effectively

GS2. Communicate clearly using technical terminology: both verbally and in written form- for documenting procedures, reporting outcomes, and presenting project results

GS3. Work efficiently in multidisciplinary teams within cleanroom and lab environments, coordinating with engineers, technicians, and quality personnel.

GS4. Follow strict protocols in cleanroom environments with high accuracy and care, ensuring consistency and quality in high-precision fabrication steps.

GS5. Stay updated with advancements in semiconductor technology, tools, and materials: demonstrate flexibility in learning and applying new methods and systems.

Annexure VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

Elements	Assessment Criteria for Performance Criteria/Learning Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
Introduction to Semiconductor Fabrication	**PC1.** student can explain the fundamental concepts of semiconductor physics, including energy bands and charge carriers. **PC2.** Student can compare the electrical, optical, and thermal properties of silicon and III-V compounds. **PC3**. Student can describe the importance of a cleanroom in semiconductor manufacturing and Identify different cleanroom classifications and contamination control measures.	5	3	-	-
Wafer Manufacturing and Preparation	**PC4**. Student can describe the wafer slicing process, including the use of diamond wire saws and its impact on wafer thickness and material loss **PC5**. Student can explain Techniques and Applications of Epitaxial Growth **PC6**. Student can explain the principles and processes of the Czochralski and Float-Zone methods for crystal growth and Demonstrate understanding of factors affecting crystal quality, such as temperature control, rotation speed, and impurity levels.	7	3	-	-
Photolithography and Patterning	**PC7.** Theory: • Fundamentals of Photolithography: Light Sources, Masks, and Photoresists • Process Steps: Spin Coating, Exposure, Development, and Hard Bake • Advanced Lithography Techniques and Applications **PC8.** practical: • Hands-on Lithography Process: Spin Coating to Development • Mask Alignment and Pattern Transfer Exercises	5	4	-	-
Etching Techniques	**PC9**. Theory : • Introduction to Etching: Wet etching • -Isotropic vs. Anisotropic Etching and Selectivity Control • Plasma-Based Dry Etching: Reactive Ion Etching (RIE), Inductively Coupled Plasma	5	4	-	-

	(ICP) • Advanced Etching Techniques: Deep Reactive Ion Etching (DRIE) • -Wet vs. Dry Etching **PC10**. Practical : • Demonstration: Wet and Dry Etching • Demonstration: Etch Profile Analysis and Process Optimization				
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Doping and Diffusion Processes	**PC13**. Theory : Fundamentals of Doping: Ion Implantation and Diffusion ; Dopant Profiles and Activation Techniques ; High-Temperature Annealing Processes and Rapid Thermal Annealing (RTA) ; Applications of Doping in Device Fabrication: p-n Junctions, Transistors **PC14**. Practical : Demonstration: Ion Implantation and Annealing Processes ;Demonstration: Doping Profile Characterization	6	4	-	-
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Chemical Mechanical Planarization (CMP)	**PC19**. Theory : Principles of CMP: Material Removal, Planarization, and Surface Smoothing ; CMP Slurries and Pads: Composition and Selection Criteria ; Applications of CMP in Semiconductor Fabrication: Interlayer Dielectrics, Metal Layers; Challenges in CMP: Dishing, Erosion, Defectivity	10	5	-	-

	PC20. Practical Demonstration: CMP Process ;Demonstration: Surface Planarity and Roughness Measurement				
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Process Integration and Yield Management	**PC25**: Theory: Integration of Fabrication Processes: Process Flow Design and Optimization; Yield Management and Defect Reduction Techniques; Statistical Process Control (SPC) and Process Monitoring; Future Trends in Semiconductor Fabrication: Advanced Nodes, 3D Integration **PC26**. Practical: Demonstration: Process Integration Case Study; Demonstration: Yield Analysis and Process Optimization	10	6	-	-
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Final Project and Process Optimization	**PC29**. Practical: Final Project: Design and Implementation of a Semiconductor Fabrication Process; Project Presentation and Evaluation	-	-	20	-
Viva	Include all Elements	-	-	-	20
Grand Total		**100**	**60**	**20**	**20**

Annexure VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. Competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service, or technology.