QUALIFICATION FILE – Standalone NOS

Essentials of High-Level Synthesis Programming and Accelerator Design

☐ Horizontal/Generic ☐ Vertical/Specialization

☒ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☒ OEM

NCrF/NSQF Level: 5

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

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Section 1: Basic Details

1.	**NOS-Qualification Name**	**Essentials of High-Level Synthesis Programming and Accelerator Design**	
2.	**Sector/s**	Electronics	
3.	**Type of Qualification ☒ New ☐ Revised**	**NQR Code & version of the existing /previous qualification: NA**	**Qualification Name of the existing/previous version: NA**
4.	**National Qualification Register (NQR) Code & Version** *(Will be issued after NSQC approval.)*	NG-05-EH-02910-2024-V1-NIELIT	**5. NCrF/NSQF Level: 5**
6.	**Brief Description of the Standalone NOS**	The standalone (NOS) covers a comprehensive range of essential topics in digital circuit and system implementation using C/C++ and High-Level Synthesis (HLS) tools. It begins with an HLS introduction, encompassing design overview, flow, port definitions, propagation delay computation, and management of functions and data flow. The syllabus advances to sequential circuit design methodologies, including single-cycle IP-centric approaches for parallel and serial conversions, state machine implementation, timers, counters, debounce circuits, clock generators, and edge detectors.	
7.	**Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee**	**a. Entry Qualification & Relevant Experience:**	

S. No.	Academic/Skill Qualification (with Specialization - if applicable)	Relevant Experience (with Specialization - if applicable)
1	2nd year of UG in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	NA
2	3 Years of Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 10th	1.5 Years
3	2 Year of diploma in Electronics and Communication Engineering/	NA

	Electrical Engineering/CS/IT/Physics/Electronics and allied branches after class 12th	
4	NSQF Level 4.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years
5	NSQF Level 4 Electronics and Communication Engineering/ Electrical Engineering/CS/IT/Physics/Electronics and allied branches	1.5 Years

b. Age: 18 Years

8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	2 Credits	**9. Common Cost Norm Category (I/II/III)** *(wherever applicable)***:** Category-I
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA	
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☒**Offline** ☐ **Online** ☐ **Blended**	

Training Delivery Mode	Theory (Hours)	Practical (Hours)	Total (Hours)
Classroom (offline)	30	30	60

The mode of delivery shall be based on the regional demand and can be offered in anyof the above modes mentioned.

12. Assessment Criteria

Theory (Marks)	Practical (Marks)	Project/ Presentation /Assignment (Marks)	Viva/ Internal Assessment (Marks)	Total (Marks)	Passing %age
100	60	20	20	200	50%

The centralized online assessment is conducted by the Examination Wing, NIELIT Headquarters.

13.	**Is the NOS Amenable to Persons with Disability**	☒ **Yes** ☐ **No If "Yes", specify applicable type of Disability:** **a)** Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims **b)** Visual Impairment: Low Vision	
14.	**Progression Path After Attaining the Qualification, wherever applicable** *(Please show Professional and Academic progression)*	Design/Application Engineer/Team Lead / Project Manager	
15.	**How participation of women will be encouraged?**	Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women's participation under other schemes launched by the Government from time to time.	
16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	Qualification files available in English & Hindi Language	
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	Name: Jayaraj U Kidav Email: jayaraj@nielit.gov.in Website: https://nielit.gov.in/ Name: Ishant Kumar Bajpai Email: ishant@nielit.gov.in Website: https://nielit.gov.in/ Name: Deepam Dubey Email: deepamdubey@nielit.gov.in Website: https://nielit.gov.in/ Name: Sreejeesh S.G Email: sreejeesh@nielit.gov.in Website: https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI Design
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI Design
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No Available at Annexure-II
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B. Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech.

4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted
5.	**Tools and Equipment Required for Assessment**	Same as for training ☒ Yes ☐ No

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided: 7
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure:** Industry Validation	*Available at* Annexure-III: Industry Validation
4.	**Annexure:** Training Details	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning
6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	• Develop proficiency in combinational and sequential circuit design, encompassing concepts like loop unrolling and interface synthesis. • Acquire knowledge about state machine implementation and single-cycle design flow for sequential circuits. • Gain an in-depth understanding of OpenCL concepts, including kernel execution models, loop transformations, and data/memory dependency management.	• The job role/outcomes relate to Professional Theoretical Knowledge/Process by ensuring a deep understanding of HLS design principles, enabling the creation of efficient combinational and sequential circuits. • Knowledge of state machine theory and interface synthesis lays the foundation for robust digital system design.	5
Professional and Technical Skills/ Expertise/ Professional Knowledge	• Proficiency in using HLS tools for designing and simulating combinational and sequential circuits, including advanced techniques like loop unrolling, function pipelining. • Mastery of FPGA-based function acceleration, including OpenCL kernel execution, loop optimizations, memory partitioning, and efficient data transfer techniques, ensuring high-performance hardware designs.	• The outcomes align with Professional and Technical Skills by equipping candidates with expertise in HLS tools and techniques for designing and simulating combinational and sequential circuits, ensuring optimized resource usage. Mastery of FPGA-based acceleration through OpenCL and advanced loop optimizations enables high-performance and scalable hardware solutions.	5
Employment Readiness & Entrepreneurship **Skills & Mind-set/Professional Skill**	• This entrepreneurial skill set empowers candidates to not only seek employment but also pursue opportunities in startups or tech ventures focused on hardware acceleration solutions. • This technical expertise ensures candidates can develop efficient hardware designs that meet industry standards, enhancing their employability in the semiconductor and embedded systems sectors.	• The job role/outcomes emphasize essential technical skills that enhance employment readiness in the rapidly evolving tech industry. Mastery of high-level synthesis and circuit design not only prepares candidates for immediate job opportunities but also fosters an entrepreneurial mindset by equipping them with the ability to innovate	5

		and develop competitive solutions.	
Broad Learning Outcomes/Core Skill	• Capability to analyze propagation delays, manage conditional statements, and apply techniques like loop unrolling and pipelining to improve circuit performance and efficiency. • Demonstrate practical skills in FPGA-based implementation using OpenCL, mastering concepts like kernel execution, memory optimization, and advanced parallel processing techniques.	• The job role aligns with Broad Learning Outcomes/Core Skills by emphasizing the ability to design and optimize digital circuits using High-Level Synthesis (HLS), enabling resource-efficient hardware implementation. It fosters strong analytical skills to troubleshoot and refine performance through techniques like pipelining, loop unrolling, and latency optimization.	5
Responsibility	Candidates must take ownership of designing and implementing combinational and sequential circuits using high-level synthesis (HLS) techniques, ensuring that all designs meet specified performance criteria and industry standards. Candidates should actively engage in the continuous improvement of existing designs by analyzing performance metrics and implementing optimizations such as loop unrolling, pipelining, and resource management.	The job role outcomes related to Combination Circuits and Sequential Circuits Design emphasize the responsibility of ensuring high-quality design and implementation of digital systems, which is crucial for maintaining industry standards and reliability. Candidates must be accountable for rigorous testing and validation processes, ensuring that all designs function correctly and meet specified performance metrics.	5

Annexure-II: Tools and Equipment (lab set-up)

LIST OF EQUIPMENT (For a batch of 30 students)

	Description	Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
2	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
3	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
4	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba, Medinipur	9434996748	bginfotech2007@gmail.com
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com
6	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com
7	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2024-25	500	200	20
2025-26	500	200	20
2026-27	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	☐Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
2	☐Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
3	☐Showing Practical Demonstrations to the learners	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
4	☐Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Design Software (Cadence & Xilinx) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80
5	☐Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	20:80

6	☐Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	☐On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Design Software	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. Description:

This course covers advanced techniques in High-Level Synthesis (HLS) for designing combination and sequential circuits using C/C++. Students will explore the HLS design flow, ports, and propagation delay computation, as well as develop test benches. Topics include IP-centric design flow for sequential circuits, state machines, functional pipelining, and interface synthesis. Additionally, function acceleration on FPGA will be explored through OpenCL concepts, including kernel execution, loop optimization, and memory dependencies.

2. Scope:

The scope covers the following:

The scope of this course encompasses the design and implementation of both combinational and sequential circuits using High-Level Synthesis (HLS) and C/C++. It provides in-depth knowledge of HLS design flow, test bench development, and optimization techniques for FPGA implementation. Students will also learn about function acceleration using OpenCL, focusing on loop optimization, memory dependencies, and real-time performance improvements, preparing them for advanced FPGA design roles.

3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

Combination Circuits and Test Benches using C/C++

- Able to design combinational logic circuits with C/C++ language using the HLS approach.
- Learn to work with Xilinx Vitis-HLS and Vivado suite Toolsets
- Able to generate RTL hardware IPs using Vitis-HLS

Sequential Circuits Design using HLS

- Able to use HLS concepts for designing sequential logic circuits
- Learn to Write C-testbench in HLS
- Able to optimize the design using the Interfaces

Function Acceleration on FPGA

- Understand the concepts of FPGA-Based embedded systems
- Able to accelerate compute-intensive algorithms on Zynq platforms Using C/C++/OpenCL
- Able to run the accelerated applications on FPGAs

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Expertise in developing combination circuits using C/C++, including creating robust test benches for functional validation, managing data types and conditional statements, utilizing bit precision libraries for accuracy, and optimizing designs through combinatorial loop unrolling and resource management techniques.
- Proficiency in HLS for sequential circuit design, covering single-cycle methodologies and IP-centric flows for parallel-to-serial and serial-to-parallel conversions, alongside implementing state machines, timers, counters, debounce circuits, clock generators for precise timing, and functional pipelining with interface synthesis to optimize performance and integration of complex designs.
- Proficiency in OpenCL concepts for FPGA acceleration, emphasizing kernel execution models, and efficient data transfer strategies, loop latency optimization, array partitioning, loop merging, pipeline implementation, and resolving data and memory dependencies to enhance FPGA computational efficiency in function acceleration applications.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1. Proficiency in programming combination circuits and developing robust test benches using C/C++ for functional verification.

GS2. Ability to utilize HLS for sequential circuit design, including single-cycle methodologies and IP-centric flows for parallel and serial data processing.

GS3. Competence in optimizing designs through techniques such as combinatorial loop unrolling, managing overloading, and addressing resource constraints.

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project Marks	Viva Marks
Essentials of High-level synthesis programming and Accelerator design	**Combination Circuits and Test Benches using C/C++**	30	20	-	6
	• Able to design combinational logic circuits with C/C++ language using the HLS approach	-	-	-	-
	• Learn to work with Xilinx Vitis-HLS and Vivado suite Toolsets	-	-	-	-
	• Able to generate RTL hardware IPs using Vitis-HLS	-	-	-	-
	Sequential Circuits Design using HLS	30	20	-	7
	• Able to use HLS concepts for designing sequential logic circuits	-	-	-	-
	• Learn to Write C-testbench in HLS	-	-	-	-
	• Able to optimize the design using the Interfaces	-	-	-	-
	Function Acceleration on FPGA	40	20	-	7
	• Understand the concepts of FPGA-Based embedded systems	-	-	-	-
	• Able to accelerate compute-intensive algorithms on Zynq platforms Using C/C++/OpenCL	-	-	-	-
	• Able to run the accelerated applications on FPGAs	-	-	-	-
	Total Marks -200	**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym:

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary:

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.