QUALIFICATION FILE – Standalone NOS

Fundamentals of VLSI Design

☐ Horizontal/Generic ☐ Vertical/Specialization

☐ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☒ OEM

NCrF/NSQF Level: 4

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY

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Section 1: Basic Details

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<tr><td>2.</td><td>Sector/s</td><td colspan="2">Electronics</td></tr>
<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version (Will be issued after NSQC approval.)</td><td>NG-04-EH-02901-2024-V1-NIELIT</td><td>5. NCrF/NSQF Level: 4</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">This Standalone NOS provides a comprehensive overview of its evolution and critical role in modern electronics, covering CMOS transistor theory, MOSFET operation principles, scaling trends, and semiconductor manufacturing advancements. It explores CMOS inverter characteristics, CMOS logic design with fundamental gates and advanced combinational logic techniques, and transistor-level schematics. The course also addresses on-chip wire modeling, packaging technologies, gate delays, logical effort analysis for optimal designs, and timing considerations in sequential circuits, emphasizing setup, hold time analysis, and performance optimization strategies.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
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<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Relevant Experience (with Specialization - if applicable)</th></tr>
<tr><td>1</td><td>12th or equivalent in Science with Physics and Maths</td><td>NA</td></tr>
<tr><td>2</td><td>2 Years of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches after class 10th</td><td>NA</td></tr>
<tr><td>3</td><td>NSQF Level 3.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches</td><td>1.5 Years</td></tr>
<tr><td>4</td><td>NSQF Level 3 in Electronics and Communication Engineering/ Electrical</td><td>1.5 Years</td></tr>
</table></td></tr>
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		Engineering/CS/IT and allied branches **b. Age**: 18 Years
8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	2 Credits **9. Common Cost Norm Category (I/II/III)** *(wherever applicable)***:** **Category-I**
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☒**Offline** ☐ **Online** ☐ **Blended** **Training Delivery Mode** / **Theory (Hours)** / **Practical (Hours)** / **Total (Hours)** **Classroom (offline)** / 30 / 30 / 60 The mode of delivery shall be based on the regional demand and can be offered in any of the above modes mentioned. *(Refer Blended Learning Annexure-V for details)*
12.	**Assessment Criteria**	**Theory (Marks)** / **Practical (Marks)** / **Project/ Presentation /Assignment (Marks)** / **Viva/ Internal Assessment (Marks)** / **Total (Marks)** / **Passing %age** **100** / **60** / **20** / **20** / **200** / **50** The centralised online assessment is conducted by the Examination Wing, NIELIT Headquarters.
13.	**Is the NOS Amenable to Persons with Disability**	☒ **Yes** ☐ **No If "Yes", specify applicable type of Disability:** **a.** Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims **b.** Visual Impairment: Low Vision

14.	**Progression Path After Attaining the Qualification, wherever applicable** *(Please show Professional and Academic progression)*	Design/Application Engineer/Team Lead / Project Manager	
15.	**How participation of women will be encouraged?**	Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women's participation under other schemes launched by the Government from time to time.	
16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	Qualification files available in English & Hindi Language.	
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No** **URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	**Name:** Jayaraj U Kidav **Email:** jayaraj@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Ishant Kumar Bajpai **Email:** ishant@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Deepam Dubey **Email:** deepamdubey@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Sreejeesh S.G **Email:** sreejeesh@nielit.gov.in **Website:** https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 Years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No *(If "Yes", details to be provided in Annexure)*
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B.Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech
4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted

5.	**Tools and Equipment Required for Assessment**	☒ Same as for training ☐ Yes ☐ No *(details to be provided in Annexure-if it is different for Assessment)*

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided: 7
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure: Industry Validation**	*Available at* Annexure-III: Industry Validation
4.	**Annexure: Training Details**	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning

6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	• Understand the significance of VLSI technology and its application in modern electronics and explore the complete VLSI design flow, encompassing both front-end and back-end processes. • Master the principles of CMOS transistor operation and its characteristics. • Learn CMOS logic design techniques, including the design of basic gates and complex logic functions. • Gain expertise in transistor-level schematics and layout strategies. • Explore critical aspects such as on-chip wire modeling, gate delays, logical effort analysis, and optimization techniques for both combinational and sequential circuits.	1. Possesses specialized operational knowledge and understanding of VLSI technology's theoretical aspects. 2. Applies concepts in real-world electronics design scenarios, aligning with time and quality considerations for embedded systems and complex circuitry.	**4**
Professional and Technical Skills/ Expertise/ Professional	• Gain a comprehensive understanding of VLSI technology fundamentals and its critical role in modern electronics, encompassing the entire design flow from front-end design specification and verification to back-end physical design and	1. Demonstrates advanced technical skills and clarity in VLSI technology and design principles.	**4**

Knowledge	fabrication processes. • Acquire expertise in MOSFET operation principles, characteristics, and scaling trends, alongside proficiency in designing CMOS inverters, basic logic gates, and complex logic functions, optimizing circuit performance through strategic inverter sizing, noise margin analysis, and power consumption considerations. • Develop advanced skills in transistor-level schematics, layout techniques, and design rules to implement circuits efficiently, while also delving into on-chip wire modeling to grasp wire parasitics' influence on circuit performance, and apply gate delay modeling, logical effort analysis, and timing optimization strategies across combinational and sequential logic circuits to ensure superior performance and reliability.	2. Collects and interprets design data effectively, drawing critical conclusions to ensure functional and efficient outcomes.	
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	• Acquire knowledge of the complete VLSI design flow, covering both front-end (specification, design, verification) and back-end (physical design, layout, fabrication) processes. • Gain expertise in MOSFET operation fundamentals, characteristics, and scaling trends, while developing proficiency in designing CMOS inverters, basic logic gates (AND, OR, NAND, NOR), and complex logic functions. Optimize circuit performance through effective inverter sizing, comprehensive noise margin analysis, and strategic management of power consumption considerations. • Acquire proficiency in transistor-level design techniques, schematic creation, and layout considerations.	1. Demonstrates entrepreneurial mindset by identifying optimization opportunities in design, promoting efficient resource use and innovation. 2. Uses advanced tools with proficiency and manages social and emotional skills effectively to support collaborative environments.	**4**
Broad Learning Outcomes/Core Skill	• Ability to independently develop the logic required for performing VLSI design and verification tasks. • Good logical and mathematical skills, alongside an understanding of the social, political, and natural environment for organizing information and communication effectively.	1. Displays strong problem-solving and critical thinking skills essential for VLSI design, ensuring that outcomes align with industry standards and complex specifications. 2. Core skills in logic, mathematics, and	**4**

		technical presentation underpin all VLSI design tasks.	
Responsibility	Ability to manage the system resources most effectively by appropriate planning, estimation, coordination and control of the activities involved in the design & development of any task/project	1. Takes complete responsibility for the quality and timeliness of their output and those of the subordinates. 2. Shares accountability for collaborative and group projects.	**4**

Annexure-II: Tools and Equipment (lab set-up)

List of Tools and Equipment

Batch Size: 30

	Description	Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB

			Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Classroom Aids

The aids required to conduct sessions in the classroom are:

1. LCD Projector/Smart Board

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba, Medinipur	9434996748	bginfotech2007@gmail.com
2	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
3	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
4	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad,	7879982075	teena.panthi@aisect.org

				Hydrabad-500020		
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com
6	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com
7	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2025-26	500	200	20
2026-27	500	200	20
2027-28	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
2	Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30

3	Showing Practical Demonstrations to the learners	Through Virtual Simulation Software (Proteus- VSM) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
4	Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Simulation Software (Proteus- VSM) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
5	Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
6	Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Simulated Platform	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. **Description:**

VLSI Fundamentals provides a comprehensive overview of essential concepts in VLSI design, starting with an introduction to VLSI design principles and CMOS transistor theory. Participants will gain insights into CMOS inverter characteristics, logic design, and the intricacies of transistor-level schematics, layouts, and on-chip wire modeling. The course further delves into gate delay modeling, logical effort analysis, critical path optimization techniques, and timing analysis for sequential circuits. By the end of this course, participants will have a solid understanding of key fundamentals in VLSI design necessary for developing efficient and high-performance integrated circuits.

2. Scope:

The scope covers the following:

The scope of the course on VLSI Fundamentals is to provide a comprehensive understanding of the essential principles and practices in VLSI design. It covers various aspects crucial for designing integrated circuits, starting with an introduction to VLSI design principles and an in-depth exploration of CMOS transistor theory. Participants will learn about CMOS inverter characteristics and logic design, gaining insights into how to design basic logic gates and complex logic functions using CMOS technology.

3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

PC1. Introduction to VLSI Design & CMOS Transistor Theory

- Describe the evolution and significance of VLSI technology, highlighting its impact on modern electronics and computing.
- Outline and differentiate between front-end and back-end VLSI design processes, and define MOSFET, explaining its operation principles and modes (cut-off, triode, saturation) along with their significance.

PC2. CMOS Inverter Characteristics and Logic Design

- Describe the functionality and design of CMOS implementations for basic logic gates (AND, OR, NAND, NOR), and design and analyze combinational logic circuits using CMOS gates, focusing on performance metrics.
- Explain factors influencing inverter sizing and apply optimization techniques for performance and power consumption improvements, and combine basic CMOS gates to implement and optimize complex logic functions for speed or area efficiency.

PC3. Transistor Scematic, Layouts & On-chip wire modeling

- Develop transistor-level schematics for basic circuits and apply layout techniques to ensure manufacturability and performance, evaluating the impact of layout on circuit performance.
- Explain design rules for different process nodes, optimize metal layer usage and interconnect routing for performance, and apply design rules and guidelines for efficient layout.

PC4. Gate Delay, Logical Effort, Critical Path Optimization and Timing analysis for Sequential circuits

- Calculate gate delays based on MOSFET parameters, predict gate delays at different process nodes and operating conditions, and optimize logic gate designs for a balance between delay and power consumption using P/N ratio analysis.
- Define logical effort and its relevance in circuit design, apply logical effort principles to estimate delay and power consumption, identify critical paths in combinational logic circuits, and apply gate sizing and logic restructuring techniques to optimize critical paths.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Understanding the significance of VLSI technology and its role in modern electronics.
- Analyzing noise margin and power consumption considerations in CMOS circuits.
- Understanding schematic design, layout considerations, and design rules for integrated circuits.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1. Participants will hone their ability to analyze complex problems and devise solutions in VLSI design by understanding the significance of VLSI technology and the design flow. They will learn to apply critical thinking skills to evaluate noise margin, power consumption, and optimization techniques in CMOS inverter characteristics, logic design, and critical path optimization.

GS2. Learners will gain proficiency in using design tools and techniques essential for VLSI design, such as schematic design, layout considerations, and simulation of on-chip wires. They will develop skills in transistor-level design techniques, gate delay modeling, and logical effort analysis, enabling them to effectively navigate the complexities of CMOS transistor theory and logic design.

GS3. Participants will enhance their communication and collaboration skills. They will learn to effectively communicate their ideas, findings, and design solutions to peers and stakeholders. Collaboration on tasks such as bonding diagram design and packaging considerations will foster teamwork and the ability to work effectively in multidisciplinary settings within the semiconductor industry.

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module Name	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project Marks	Viva Marks
NOS1: Fundamentals of VLSI Design **NOS Code: NIE/ELE/N0113**	**Introduction to VLSI Design & CMOS Transistor Theory**	**25**	**15**	**-**	**5**
	Describe the evolution and significance of VLSI technology, highlighting its impact on modern electronics and computing.	-	-	-	-
	Outline and differentiate between front-end and back-end VLSI design processes, and define MOSFET, explaining its operation principles and modes (cut-off, triode, saturation) along with their significance.	-	-	-	-
	CMOS Inverter Characteristics and Logic Design	**25**	**15**	**-**	**5**
	Describe the functionality and design of CMOS implementations for basic logic gates (AND, OR, NAND, NOR), and design and analyze combinational logic circuits using CMOS gates, focusing on performance metrics.	-	-	-	-
	Explain factors influencing inverter sizing and apply optimization techniques for performance and power consumption improvements, and combine basic CMOS gates to implement and optimize complex logic functions for speed or area efficiency.	-	-	-	-
	Transistor Scematic, Layouts & On-chip wire modelling	**25**	**15**	**-**	**5**
	Develop transistor-level schematics for basic circuits and apply layout techniques to ensure manufacturability and performance, evaluating the impact of layout on circuit performance.	-	-	-	-
	Explain design rules for different process nodes, optimize metal layer usage and interconnect routing for performance, and apply design rules and guidelines for efficient layout.	-	-	-	-
	Gate Delay, Logical Effort, Critical Path Optimization and Timing analysis for Sequential circuits	**25**	**15**		**5**

	Calculate gate delays based on MOSFET parameters, predict gate delays at different process nodes and operating conditions, and optimize logic gate designs for a balance between delay and power consumption using P/N ratio analysis.	-	-	-	-
	Define logical effort and its relevance in circuit design, apply logical effort principles to estimate delay and power consumption, identify critical paths in combinational logic circuits, and apply gate sizing and logic restructuring techniques to optimize critical paths.	-	-	-	-
Total Marks -200		**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.