QUALIFICATION FILE-Standalone NOS

Fundamentals of Photolithography and Mask Making

☐ Horizontal /Generic ☐ Vertical/Specialization

☐ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☐ OEM

NCrF/NSQF Level: 4.5

Submitted By:

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Table of Contents

Section 1: Basic Details

<table>
<tr><td>1.</td><td>NOS-Qualification Name</td><td colspan="2">Fundamentals of Photolithography and Mask Making</td></tr>
<tr><td>2.</td><td>Sector</td><td colspan="2">Electronics</td></tr>
<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version</td><td>NG-4.5-EH-03729-2025-V1-NIELIT</td><td>5. NCrF/NSQF Level: 4.5</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">The Standalone NOS "Fundamentals of Photolithography and Mask Making" is designed to provide foundational knowledge and practical skills required for photolithography processes and mask-making in semiconductor manufacturing. Participants will learn the principles of light exposure, photoresist application, and pattern transfer onto substrates. They will develop hands-on expertise in mask design, alignment, etching, and defect inspection. It equips learners to work in cleanroom environments, ensuring compliance with industry standards and safety protocols. It prepares individuals for roles in photolithography operations within the electronics and semiconductor industries, supporting advanced manufacturing processes.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
<table>
<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Required Experience (with Specialization - if applicable)</th></tr>
<tr><td>1.</td><td>3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th</td><td>NA</td></tr>
<tr><td>2</td><td>3rd year of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/ allied branches after class 10th</td><td>NA</td></tr>
<tr><td>3</td><td>1st year of UG in Electronics Engineering/Physics/ allied fields</td><td>NA</td></tr>
</table></td></tr>
</table>

		4	12th Pass	1.5 year experience in ESDM Sector
		5	10th pass plus 2-year NTC in relevant field of Electronics Sector	1.5-year experience in ESDM Sector
8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	**4 Credits**	**9. Common Cost Norm Category (I/II/III)** *(wherever applicable)***: Category-I**	
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA		
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	**☒Offline ☐Online ☐Blended**		

Training Delivery Modes	**Theory (Hours)**	**Practical (Hours)**	**Total (Hours)**
Classroom (offline)	**30**	**90**	**120**

12.	**Assessment Criteria**	

Theory (Marks)	**Practical (Marks)**	**Project (Marks)**	**Viva (Marks)**	**Total (Marks)**	**Passing %age**
100	**60**	**20**	**20**	**200**	**50**

The centralized online assessment is conducted by the Examination Wing, NIELIT Headquarters.
*Assessment strategy shall be as per NIELIT Norms prevailing at times.

13.	**Is the NOS Amenable to Persons with Disability**	**☒ Yes ☐ No** a. Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims b. Visual Impairment: Low Vision
14.	**Progression Path After Attaining the Qualification, wherever applicable** *(Please show Professional and Academic progression)*	MEMS Backend Fabrication Engineer -> Semiconductor Fabrication Engineer
15.	**How participation of women will be encouraged?**	Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women's participation under other schemes launched by the Government from time to time.
16.	**Other Indian languages in which the Qualification & Model**	Qualification file is available in English and Hindi languages.

	Curriculum are being submitted		
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	**☐ Yes ☒ No URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	**Name:** Sh. Sreejeesh SG **Email:** sreejeesh@nielit.gov.in **Contact No.:** 9447769756 **Website:** https://www.nielit.gov.in **Name:** Sh. Nandakumar R **Email:** nanda@nielit.gov.in **Contact No.:** 9995427802 **Website:** https://www.nielit.gov.in	
19.	**Final Approval Date by NSQC:18.02.2025**	**20. Validity Duration: 3 Years**	**21. Next Review Date: 18.02.2028**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 2 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design. Or M.Sc. in Physics/Electronics/Material Science and allied branches; with 2 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design.
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design. Or M.Sc. in Physics/Electronics/Material Science and allied branches; with 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design.
3.	**Tools and Equipment Required for Training**	☒ Yes ☐No

		Available at Annexure-II
4.	**In Case of Revised Qualification, Details of Any Upskilling Required for Trainer**	NA

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control and allied branches with 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design. Or M.Sc. in Physics/Electronics/Material Science and allied branches 3 years of relevant experience in the field of Semiconductor Manufacturing / Semiconductor Fabrication and Packaging/VLSI Design.
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online, and the paper comprise of MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I- card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech.
4.	**Assessment Mode** *(Specify the assessment mode)*	Centralized online examination will be conducted
5.	**Tools and Equipment Required for Assessment**	☒ Same as for training ☐ Yes ☐ No *(details to be provided in Annexure-if it is different for Assessment)*

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes
2.	Number of Industry validation provided: The course has been developed in collaboration with TATA Electronics to support the development of skilled manpower for the upcoming semiconductor industry.
3.	Estimated number of people to be trained: 500
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): No NIELIT is recognized as an Adjudicating Body (AB) and Assessment Body (AA) under the Government category. NIELIT is the Human Resource Development (HRD) arm of MeitY, therefore, the Line Ministry Concurrence is not required.

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF level/NSQF descriptors *(Mandatory)*	Available at Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for qualification *(Mandatory, except in case of online course)*	Available at Annexure-II: Tools and Equipment
3.	**Annexure:** Industry Validation	Available at Annexure-III: Industry Validation
4.	**Annexure: Training Details**	Available at Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case selected Mode of delivery is "Blended Learning")*	Available at Annexure-V: Blended Learning
6.	**Annexure/Supporting Document:** Standalone NOS- Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Detailed Assessment Criteria *(Mandatory)*	Available at Annexure-VII: Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	Available at Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	Available at Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum *(Mandatory – Public view)*	Available at Annexure-A: Model Curriculum

Annexure I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	• Understanding photolithography fundamentals, light sources, mask making, and process integration. • Adherence to cleanroom safety standards and operational protocols.	Operate in a predictable and routine environment by following defined procedures for lithography processes.	4.5
Professional and Technical Skills/ Expertise/ Professional Knowledge	• Knowledge of advanced photolithography tools, spin coaters, UV exposure systems, and alignment techniques. • Expertise in troubleshooting issues in mask fabrication, photoresist coating, and defect inspections.	Apply technical knowledge to operate photolithography tools and implement precise techniques for mask-making and etching processes.	4.5
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	• Perform critical steps like exposure, etching, liftoff, and photoresist optimization with minimal errors. • Ability to evaluate and improve process outcomes, ensuring high-quality outputs.	Develop technical problem-solving abilities and practical skills necessary for photolithography and semiconductor manufacturing roles.	4.5
Broad Learning Outcomes/Core Skill	• Documentation of photolithography processes, preparation of reports, and adherence to compliance standards. • Effective communication for collaboration with teams and supervisors in technical environments.	Demonstrate core skills for documenting technical details, reporting defects, and communicating results effectively within a professional setup.	4.5
Responsibility	• Responsible for independently executing photolithography steps like spin coating, exposure, etching, and mask inspections. • Ensure precision, quality control, and adherence to project requirements	Perform tasks independently while taking accountability for quality outcomes and adhering to cleanroom and safety standards.	4.5

Annexure II: Tools and Equipment (Lab Set-Up)

List of Tools and Equipment

Sl. No	Description	Qty.	Specifications
1	Classroom	1	30 Sq. m
2	Student Chair	30	-
3	Student Table	30	-
4	LCD Projector	1	-
5	Trainer Chair & Table	1	-
6	Pin up Board	1	-
7	White Board	1	-
8	Desktop Computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB
9	Desk jet printer	1	A4

Cleanroom Facilities

- Cleanroom Environment (Class 100 or Class 1000)
- Air Showers
- Sticky Mats
- Cleanroom Attire (Gowns, Gloves, Shoe Covers, Face Masks, Hairnets)

Photolithography Tools

1. Light Sources
    - UV Light Source
    - Deep UV (DUV) Light Source
    - Extreme UV (EUV) Light Source
2. Exposure Systems
    - Contact Exposure System
    - Proximity Exposure System
    - Projection Exposure System
3. Photomasks
    - Mask Aligners
    - Photomask Inspection Tools
    - Electron Beam Lithography System (For Mask Making)
4. Spin Coating Tools
    - Spin Coaters (For Photoresist Application)

- Photoresist Thickness Measurement Tools

5. Baking Tools
   - Prebake Oven
   - Post-Bake Oven

Etching Tools
- Wet Etching Benches
- Dry Etching Systems (e.g., Reactive Ion Etching - RIE)
- Plasma Etching Systems

Liftoff Tools
- Liftoff Process Chambers
- Microscopes (For Inspecting Liftoff Quality)

Material Handling and Measurement Tools
- Wafer Holders
- Wafer Alignment Tools
- Critical Dimension (CD) Measurement Tools
- Profilometers

Chemical Handling Tools
- Chemical Dispensers (For Photoresist and Etching Solutions)
- Chemical Fume Hoods
- Safety Equipment (Spill Kits, Eye Wash Stations, Gloves)

Metrology and Inspection Tools
- Scanning Electron Microscope (SEM)
- Atomic Force Microscope (AFM)
- Optical Microscopes
- Particle Counters

General Equipment
- Desktop Computers with CAD Software (e.g., Cadence, Mentor Graphics)
- LCD Projector
- Pin-up Board
- Whiteboard

Consumables
- Silicon Wafers
- Photoresists (Positive and Negative)
- Cleaning Solvents (Acetone, Isopropyl Alcohol)
- Etchants
- Developer Chemicals

Annexure III: Industry Validations Summary

The course has been developed in collaboration with TATA Electronics to support the development of skilled manpower for the upcoming semiconductor industry.

Annexure IV: Training & Employment Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2025-26	**100**	**50**	**10**
2026-27	**200**	**70**	**15**
2027-28	**200**	**70**	**15**

Data to be provided year-wise for next 3 years.

Annexure V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools: NA

Annexure VI: Performance Criteria details

1. **Description:**

   The purpose of this qualification is to train individuals in the fundamentals of photolithography and mask making, enhancing their employability in industries like semiconductors, electronics manufacturing, and research and development. The aim is to provide hands-on expertise in lithographic processes, mask making, and related technologies, enabling participants to independently apply the knowledge and skills gained. Participants will gain exposure to key lithographic techniques, process optimization, and the integration of advanced tools in photolithography.

2. Scope:

The scope covers the following:

- Prepares individuals for roles in photolithography and mask making, including positions such as Lithography Technician, Mask Fabrication Specialist, and Semiconductor Process Engineer.
- Equips participants with the skills to perform critical tasks such as spin coating, exposure, etching, and mask inspection, ensuring proficiency in advanced lithographic processes used in semiconductor manufacturing.
- Extends to opportunities in the development and optimization of lithographic processes, requiring expertise in photolithography equipment, process control, and defect analysis for high-precision industries.

3. Elements and Performance Criteria

Elements	Performance Criteria
Light Sources	**PC1:** Understand the types of light sources (UV, DUV, EUV) and their impact on lithographic resolution. **PC2:** Demonstrate the calibration and setup of light sources for uniform exposure.
Exposure System	**PC3**: Explain the functionality of contact, proximity, and projection exposure systems. **PC4:** Operate exposure systems and perform alignment of masks and substrates.
Photo Masks	**PC5**: Understand the types, materials, and fabrication processes of photomasks. **PC6**: Perform inspection of photomasks for defects and propose corrective actions.
Mask Making	**PC7**: Explain the processes and materials used in mask making, including electron beam lithography. **PC8**: Fabricate a simple photomask and evaluate its quality based on resolution and alignment.
Photoresist and Spin Coating	**PC9:** Describe the properties and classifications of photoresists (positive and negative). **PC10:** Perform spin coating of photoresists and achieve desired thickness and uniformity.
Prebake Process	**PC11:** Understand the purpose and parameters (time, temperature) of the prebake process. **PC12:** Conduct prebake processes and troubleshoot common issues affecting photoresist properties.
Exposure Process	**PC13:** Explain the interaction of light with photoresist and factors affecting critical dimensions (CD). **PC14:** Optimize exposure parameters to achieve desired lithographic patterns.
Post-Bake Process	**PC15:** Describe the role and optimization of post-bake processes in lithography. **PC16**: Implement post-bake processes and evaluate their effect on photoresist development.
Etching Process	**PC17:** Explain wet and dry etching techniques and their roles in lithography. **PC18:** Perform etching processes and analyze etch profiles and selectivity.

Liftoff Process	**PC19:** Understand the liftoff process, including critical steps and its applications in semiconductor manufacturing. **PC20**: Perform liftoff techniques and evaluate the quality and yield of the process.
Final Project/Internship	**PC21:** Design and implement a photolithography process integrating mask making and other lithographic steps. **PC22**: Prepare a final report and presentation showcasing project outcomes and technical solutions.

4. Knowledge and Understanding (KU):

The individual undergoing the course needs to know and understand:

KU1: The principles and classification of cleanrooms, including ISO standards and their significance in semiconductor manufacturing.
KU2: Sources of contamination in cleanrooms, such as particulates, microorganisms, and their control mechanisms, including HEPA filtration and airflow management.
KU3: Cleanroom safety standards, protocols, and the use of personal protective equipment (PPE) to maintain safety and prevent contamination.
KU4: Cleanroom design fundamentals, including airflow, pressure control, and environmental monitoring techniques.
KU5: Handling of hazardous materials within cleanrooms, including storage, disposal, and emergency response to spills and exposure incidents.
KU6: Environmental monitoring practices, including the use of particle counters and microbial contamination measurement tools, to ensure cleanroom compliance.
KU7: Standard operating procedures (SOPs) for material transfer, equipment handling, and adherence to cleanroom protocols.
KU8: The integration of cleanroom operations into semiconductor manufacturing processes and strategies for maintaining cleanroom integrity.
KU9: Cleanroom certification requirements, including ISO standards, and the process of preparing for and passing certification audits.
KU10: Emerging trends in cleanroom technology, advanced contamination control techniques, and future challenges in cleanroom safety.

5. Generic Skills (GS):

The user/individual on the job needs to know how to:

GS1: Follow instructions, guidelines, and procedures related to photolithography processes, equipment handling, and safety standards.
GS2: Communicate effectively with team members and supervisors regarding photolithography protocols, process optimization, and defect analysis.
GS3: Apply problem-solving skills and critical thinking to troubleshoot issues in photolithographic processes, mask alignment, and pattern transfer.
GS4: Collaborate effectively in teams to complete photolithography tasks, optimize workflows, and ensure quality outcomes.

Annexure VII: Assessment Criteria

Detailed assessment criteria for each NOS/Module are as follows:

Elements	Assessment Criteria for Performance Criteria/Learning Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
Light Sources	**PC1:** Understand the types of light sources (UV, DUV, EUV) and their impact on lithographic resolution. **PC2:** Demonstrate the calibration and setup of light sources for uniform exposure.	10	6	-	-
Exposure System	**PC3**: Explain the functionality of contact, proximity, and projection exposure systems. **PC4:** Operate exposure systems and perform alignment of masks and substrates.	10	6	-	-
Photo Masks	**PC5**: Understand the types, materials, and fabrication processes of photomasks. **PC6**: Perform inspection of photomasks for defects and propose corrective actions.	10	6	-	-
Mask Making	**PC7**: Explain the processes and materials used in mask making, including electron beam lithography. **PC8**: Fabricate a simple photomask and evaluate its quality based on resolution and alignment.	10	6	-	-
Photoresist and Spin Coating	**PC9:** Describe the properties and classifications of photoresists (positive and negative). **PC10:** Perform spin coating of photoresists and achieve desired thickness and uniformity.	10	6	-	-
Prebake Process	**PC11:** Understand the purpose and parameters (time, temperature) of the prebake process. **PC12:** Conduct prebake processes and troubleshoot common issues affecting photoresist properties.	10	6	-	-
Exposure Process	**PC13:** Explain the interaction of light with photoresist and factors affecting critical dimensions (CD). **PC14:** Optimize exposure parameters to achieve desired lithographic patterns.	10	6	-	-
Post-Bake Process	**PC15:** Describe the role and optimization of post-bake processes in lithography.	5	6	-	-

	PC16: Implement post-bake processes and evaluate their effect on photoresist development.				
Etching Process	**PC17:** Explain wet and dry etching techniques and their roles in lithography. **PC18:** Perform etching processes and analyze etch profiles and selectivity.	15	6	-	-
Liftoff Process	**PC19:** Understand the liftoff process, including critical steps and its applications in semiconductor manufacturing. **PC20**: Perform liftoff techniques and evaluate the quality and yield of the process.	10	6	-	-
Final Project/Internship	**PC21:** Design and implement a photolithography process integrating mask making and other lithographic steps. **PC22**: Prepare a final report and presentation showcasing project outcomes and technical solutions.	-	-	20	-
Viva	Including all Elements	-	-	-	20
GRAND TOTAL		**100**	**60**	**20**	**20**

Annexure VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. Competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.