QUALIFICATION FILE – Standalone NOS

Fundamentals of FPGA Architecture and Programming

☐ Horizontal/Generic ☐ Vertical/Specialization

☒ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☒ OEM

NCrF/NSQF Level: 4

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

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<tr><td>2.</td><td>Sector/s</td><td colspan="2">Electronics</td></tr>
<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version (Will be issued after NSQC approval.)</td><td>NG-04-EH-02904-2024-V1-NIELIT</td><td>5. NCrF/NSQF Level: 4</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">This Standalone NOS provides a comprehensive exploration of Field-Programmable Gate Arrays (FPGAs) and their applications in digital design. Students delve into FPGA internal architecture, covering components such as Look-Up Tables (LUTs), flip-flops, and interconnect. The curriculum focuses on FPGA design techniques using Hardware Description Languages (HDLs) like Verilog, emphasizing syntax, data types, and RTL coding specific to FPGAs. The module introduces students to design constraints and optimization techniques, including timing analysis, pipelining, and balancing area, power, and performance requirements. Additionally, students learn FPGA verification and debugging methodologies, including simulation setups, testbench development, and effective debugging strategies tailored for FPGA-based designs.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
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<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Relevant Experience (with Specialization - if applicable)</th></tr>
<tr><td>1</td><td>12th or equivalent in Science with Physics and Maths</td><td>NA</td></tr>
<tr><td>2</td><td>2 Years of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches after class 10th</td><td>NA</td></tr>
<tr><td>3</td><td>NSQF Level 3.5 in Electronics and</td><td>1.5 Years</td></tr>
</table></td></tr>
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			Communication Engineering/ Electrical Engineering/CS/IT and allied branches	
		4	NSQF Level 3 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches	1.5 Years

b. Age: 18 Years

8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	2 Credits	**9. Common Cost Norm Category (I/II/III)** *(wherever applicable)*: Category-I
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA	
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☒ **Offline Only** ☐ **Online Only** ☐ **Blended**	

Training Delivery Mode	Theory (Hours)	Practical (Hours)	Total (Hours)
Classroom (offline)	**30**	**30**	**60**

The mode of delivery shall be based on the regional demand and can be offered in any of the above modes mentioned.

(Refer Blended Learning Annexure-V for details)

12. Assessment Criteria

Theory (Marks)	Practical (Marks)	Project/ Presentation /Assignment (Marks)	Viva/ Internal Assessment (Marks)	Total (Marks)	Passing %age
100	**60**	**20**	**20**	**200**	**50**

The centralised online assessment is conducted by the Examination Wing, NIELIT Headquarters.

13.	**Is the NOS Amenable to Persons with Disability**	☒ **Yes** ☐ **No If "Yes", specify applicable type of Disability:** **a.** Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims **b.** Visual Impairment: Low Vision	
14.	**Progression Path After Attaining the Qualification, wherever applicable** *(Please show Professional and Academic progression)*	*Design/Application Engineer/Team Lead / Project Manager*	
15.	**How participation of women will be encouraged?**	Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women's participation under other schemes launched by the Government from time to time.	
16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	Qualification files available in English & Hindi Language.	
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	**Name:** Jayaraj U Kidav **Email:** jayaraj@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Ishant Kumar Bajpai **Email:** ishant@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Deepam Dubey **Email:** deepamdubey@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Sreejeesh S.G **Email:** sreejeesh@nielit.gov.in **Website:** https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 Years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI Design
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI Design
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No *(If "Yes", details to be provided in Annexure)*
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B.Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech

4.	**Assessment Mode** *(Specify the assessment mode)*	Online for Theory Online/ Offline/ Blended for other assessment components depending on the region where the assessment is conducted
5.	**Tools and Equipment Required for Assessment**	☒ Same as for training ☐ Yes ☐ No *(details to be provided in Annexure-if it is different for Assessment)*

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided: 7
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure: Industry Validation**	*Available at* Annexure-III: Industry Validation
4.	**Annexure: Training Details**	*Available at* Annexure-IV: Training Details

5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning
6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	1. Understanding the internal architecture and components of FPGAs. 2. Familiarity with FPGA applications and advantages in digital design.	Provides foundational theoretical knowledge of FPGA systems and their use in modern electronics. Enables learners to comprehend the design process.	**4**
Professional and Technical Skills/ Expertise/ Professional Knowledge	1. Writing RTL code using Verilog for FPGA designs. 2. Applying timing constraints and optimization techniques.	Learners acquire technical skills for implementing digital designs and enhancing system performance through practical optimization techniques.	**4**
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	1. Preparing for roles like FPGA design/verification engineers. 2. Fostering an innovative approach to embedded systems design.	Develops skills for entry-level positions in the semiconductor and embedded systems industry while encouraging entrepreneurship in digital design projects.	**4**

Broad Learning Outcomes/Core Skill	1. Gaining analytical skills to debug FPGA-based designs. 2. Understanding the end-to-end FPGA design flow and methodology.	Promotes logical thinking and problem-solving skills essential for efficient FPGA system development and verification.	**4**
Responsibility	1. Independently designing, testing, and debugging FPGA-based systems. 2. Ensuring compliance with design specifications, including timing, power, and resource constraints.	Learners are equipped to take responsibility for the design and functionality of FPGA systems, either working independently or collaboratively in a team.	**4**

Annexure-II: Tools and Equipment (lab set-up)

List of Tools and Equipment

Batch Size: 30

	Description	Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent

			Memory: 16GB RAM, Internal Storage: 500GB Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Classroom Aids
The aids required to conduct sessions in the classroom are:

1. LCD Projector/Smart Board

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba, Medinipur	9434996748	bginfotech2007@gmail.com
2	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
3	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com

4	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com
6	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com
7	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2024-25	500	200	20
2025-26	500	200	20
2026-27	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
2	Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
3	Showing Practical Demonstrations to the learners	Through Virtual Simulation Software (Proteus- VSM) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
4	Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Simulation Software (Proteus- VSM) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
5	Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
6	Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Simulated Platform	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. Description:

This course offers a comprehensive study of Field-Programmable Gate Arrays (FPGAs), exploring their applications and advantages in digital design. Students delve into FPGA architecture, understanding its components like Look-Up Tables (LUTs) and flip-flops. Through hands-on practice with Hardware Description Languages (HDLs) like Verilog, they learn to write RTL code tailored for FPGA implementation. The curriculum covers the FPGA design flow from entry to bitstream generation, alongside design constraints. Advanced topics include FPGA design optimization techniques, verification, and debugging strategies, ensuring proficiency in FPGA-based projects.

2. Scope:

The scope covers the following:

This course provides a comprehensive introduction to Field-Programmable Gate Arrays (FPGAs) and their significance in modern digital design. Students will gain foundational knowledge of FPGA technology, exploring its applications and the advantages that make it an adaptable solution for various design challenges. The course delves into the internal architecture of FPGAs, including critical components such as Look-Up Tables (LUTs), flip-flops, interconnects, and the diversity of FPGA families, offering a holistic understanding of the technology.

3. Elements and Performance Criteria:

To be competent, the user/individual on the job must be able to:

Introduction to FPGAs

- Explain the fundamental concepts of FPGAs and their role in digital design.
- Describe various applications of FPGAs in modern electronics.

Hardware Description Languages for FPGAs

- Demonstrate knowledge of Verilog syntax and data types.
- Write effective RTL (Register Transfer Level) code for FPGA implementations.

FPGA Design Flow and Optimization Technique

- Implement design constraints effectively to meet specified requirements.
- Apply optimization techniques such as timing analysis, pipelining, and retiming to improve FPGA performance.

FPGA Verification and Debugging

- Apply debugging techniques to identify and resolve issues in FPGA designs.
- Utilize simulation tools to ensure designs meet required specifications and performance criteria.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Develop a comprehensive understanding of FPGAs, including their applications and advantages in digital design, the internal architecture featuring components like Look-Up Tables (LUTs), flip-flops, and interconnects, as well as exploring different FPGA families and their available resources, such as memory blocks and DSP slices.
- Master the use of Hardware Description Languages (HDLs), particularly Verilog, for writing RTL code for FPGAs; comprehend the complete FPGA design flow from design entry to bit stream generation, including the role of design constraints; and learn optimization techniques like pipelining, retiming, and balancing trade-offs between area, power, and performance to improve FPGA design efficiency.
- Grasp the importance of FPGA simulation and verification by learning to write effective test benches and test vectors, and acquire debugging skills using tools and techniques such as logic analyzers and on-chip debugging tools to ensure correct and optimized functionality of FPGA designs.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1. Gain comprehensive expertise in FPGA architecture, Verilog proficiency, and the complete FPGA design process, covering design entry to bitstream generation with the application of design constraints. Develop skills in analyzing and optimizing designs using techniques like pipelining and retiming, while balancing trade-offs between area, power, and performance.

GS2. Develop proficiency in FPGA design validation through simulation, leveraging effective test benches and test vectors. Master debugging tools and techniques to ensure the accuracy and optimization of FPGA functionality. Improve problem-solving skills and attention to detail by identifying and resolving design issues throughout the development process

GS3. Develop proficiency in managing FPGA projects from inception to implementation by applying systematic design approaches. Adapt to diverse FPGA families and resources, staying abreast of advancements in technology and tools. Enhance collaboration and communication skills through effective teamwork and clear articulation of design decisions and optimization strategies.

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project Marks	Viva Marks
Fundamentals of FPGA Architecture and Programming **NOS Code: NIE/ELE/N0116**	**Introduction to FPGAs**	25	15		5
	• Explain the fundamental concepts of FPGAs and their role in digital design.	-	-	-	-
	• Describe various applications of FPGAs in modern electronics.	-	-	-	-
	Hardware Description Languages for FPGAs	25	15		5
	• Demonstrate knowledge of Verilog syntax and data types.	-	-	-	-
	• Write effective RTL (Register Transfer Level) code for FPGA implementations.	-	-	-	-
	FPGA Design Flow and Optimization Technique	25	15		5
	• Implement design constraints effectively to meet specified requirements.	-	-	-	-
	• Apply optimization techniques such as timing analysis, pipelining, and retiming to improve FPGA performance.	-	-	-	-
	FPGA Verification and Debugging	25	15		5
	• Apply debugging techniques to identify and resolve issues in FPGA designs.	-	-	-	-
	• Utilize simulation tools to ensure designs meet required specifications and performance criteria.	-	-	-	-
Total Marks -200		**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.