QUALIFICATION FILE – Standalone NOS

Essentials of VLSI Circuits Timing Analysis

☐ Horizontal/Generic ☐ Vertical/Specialization

☒ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☒ OEM

NCrF/NSQF Level: 4

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY (NIELIT)

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Section 1: Basic Details

<table>
<tr><td>1.</td><td>NOS-Qualification Name</td><td colspan="2">Essentials of VLSI Circuits Timing Analysis</td></tr>
<tr><td>2.</td><td>Sector/s</td><td colspan="2">Electronics</td></tr>
<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version (Will be issued after NSQC approval.)</td><td>NG-04-EH-02903-2024-V1-NIELIT</td><td>5. NCrF/NSQF Level: 4</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">This standalone NOS provides comprehensive knowledge and practical skills in timing analysis and optimization. Students will learn the fundamentals of STA, covering topics such as timing analysis principles, setup and hold timing considerations in combinational and sequential circuits, and techniques for mitigating setup and hold time violations. The module also includes methods for enhancing timing performance through pipeline stages, retiming strategies, and clock skew management.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
<table>
<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Relevant Experience (with Specialization - if applicable)</th></tr>
<tr><td>1</td><td>12th or equivalent in Science with Physics and Maths</td><td>NA</td></tr>
<tr><td>2</td><td>2 Years of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches after class 10th</td><td>NA</td></tr>
<tr><td>3</td><td>NSQF Level 3.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches</td><td>1.5 Years</td></tr>
<tr><td>4</td><td>NSQF Level 3 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches</td><td>1.5 Years</td></tr>
</table>
b. Age: 18 Years</td></tr>
</table>

<table>
<tr><td>8.</td><td>Credits Assigned to this NOS-Qualification, Subject to Assessment (as per National Credit Framework (NCrF))</td><td>2 Credits</td><td>9. Common Cost Norm Category (I/II/III) (wherever applicable):
Category-I</td></tr>
<tr><td>10.</td><td>Any Licensing Requirements for Undertaking Training on This Qualification (wherever applicable)</td><td colspan="2">NA</td></tr>
<tr><td>11.</td><td>Training Duration by Modes of Training Delivery (Specify Total Duration as per selected training delivery modes and as per requirement of the qualification)</td><td colspan="2">☒ Offline Only ☐ Online Only ☐ Blended
<table>
<tr><th>Training Delivery Mode</th><th>Theory (Hours)</th><th>Practical (Hours)</th><th>Total (Hours)</th></tr>
<tr><td>Classroom (offline)</td><td>30</td><td>30</td><td>60</td></tr>
</table>
The mode of delivery shall be based on the regional demand and can be offered in any of the above modes mentioned.

(Refer Blended Learning Annexure-V for details)</td></tr>
<tr><td>12.</td><td>Assessment Criteria</td><td colspan="2">
<table>
<tr><th>Theory (Marks)</th><th>Practical (Marks)</th><th>Project/ Presentation /Assignment (Marks)</th><th>Viva/ Internal Assessment (Marks)</th><th>Total (Marks)</th><th>Passing %age</th></tr>
<tr><td>100</td><td>60</td><td>20</td><td>20</td><td>200</td><td>50</td></tr>
</table>
The centralised online assessment is conducted by the Examination Wing, NIELIT Headquarters.</td></tr>
<tr><td>13.</td><td>Is the NOS Amenable to Persons with Disability</td><td colspan="2">☒ Yes ☐ No If “Yes”, specify applicable type of Disability:
a. Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims
b. Visual Impairment: Low Vision</td></tr>
<tr><td>14.</td><td>Progression Path After Attaining the Qualification, wherever applicable (Please show Professional and Academic progression)</td><td colspan="2">Design/Application Engineer/Team Lead / Project Manager</td></tr>
<tr><td>15.</td><td>How participation of women will be encouraged?</td><td colspan="2">Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women’s participation under other schemes launched by the Government from time to time.</td></tr>
</table>

16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	Qualification files available in English & Hindi Language.	
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No** **URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	**Name:** Jayaraj U Kidav **Email:** jayaraj@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Ishant Kumar Bajpai **Email:** ishant@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Deepam Dubey **Email:** deepamdubey@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Sreejeesh S.G **Email:** sreejeesh@nielit.gov.in **Website:** https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 Years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI Design
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI Design
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No *(If "Yes", details to be provided in Annexure)*
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B.Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech
4.	**Assessment Mode** *(Specify the assessment mode)*	Online for Theory Online/ Offline/ Blended for other assessment components depending on the region where the assessment is conducted
5.	**Tools and Equipment Required for Assessment**	☒ Same as for training ☐ Yes ☐ No *(details to be provided in Annexure-if it is different for Assessment)*

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided: 7
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure: Industry Validation**	*Available at* Annexure-III: Industry Validation
4.	**Annexure: Training Details**	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning
6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria	*Available at* Annexure-VII: Detailed Assessment Criteria

	(Mandatory)	
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	1. Gain a thorough understanding of Static Timing Analysis (STA), covering combinational and sequential circuit timing, setup and hold timing, and timing constraints for synthesis. 2. Learn about practical timing challenges such as setup and hold time violations and methods for resolution. 3. Understand timing performance improvement techniques such as pipelining and retiming, as well as clock skew adjustments.	1. Demonstrates a comprehensive understanding of STA fundamentals, essential for accurate VLSI circuit timing analysis. 2. Applies theoretical timing knowledge in real-world contexts to enhance circuit reliability and performance.	**4**
Professional and Technical Skills/ Expertise/ Professional Knowledge	1. Develop skills in using EDA tools for conducting STA, analyzing timing paths, and addressing timing issues. 2. Gain expertise in block-level and chip-level timing analysis to ensure design meets timing integrity. 3. Acquire practical experience in executing ECO flows and ensuring timing closure post-synthesis and place-and-route stages.	1. Applies technical expertise in STA and ECO workflows, essential for verifying timing closure in VLSI designs. 2. Demonstrates the ability to perform timing analysis at multiple design levels, ensuring accuracy in timing integrity.	**4**
Employment Readiness & Entrepreneurship **Skills & Mind-set/Professional Skill**	1. Develop problem-solving skills necessary for identifying and resolving setup and hold time violations in VLSI circuits. 2. Gain competency in handling timing constraints and optimization for synthesis using EDA tools.	1. Prepares participants to address timing challenges in a professional setting by optimizing circuit timing for efficient operation. 2. Demonstrates readiness to meet	**4**

	3. Acquire skills in analyzing and adjusting timing metrics, including clock skew, to enhance circuit reliability.	industry standards in timing analysis and STA practices.	
Broad Learning Outcomes/Core Skill	1. Develop expertise in STA essentials, timing path analysis, and timing report interpretation using EDA tools. 2. Understand the impact of timing constraints on synthesis and design optimization, enabling efficient timing closure. 3. Gain proficiency in block-level and chip-level timing analysis techniques, addressing timing performance challenges and ensuring design accuracy.	1. Establishes a core foundation in STA, equipping participants with industry-relevant timing skills for VLSI circuits. 2. Demonstrates the ability to conduct comprehensive timing analysis across multiple design stages.	**4**
Responsibility	Conduct thorough STA at both block and chip levels, including setup and hold time verification, timing constraint implementation, and timing closure verification.	1. Takes responsibility for maintaining timing integrity through ECO adjustments and STA. 2. Ensures adherence to timing requirements for successful circuit implementation.	**4**

Annexure-II: Tools and Equipment (lab set-up)

List of Tools and Equipment

Batch Size: 30

	Description	Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Classroom Aids

The aids required to conduct sessions in the classroom are:

1. LCD Projector/Smart Board

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba, Medinipur	9434996748	bginfotech2007@gmail.com
2	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
3	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
4	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com
6	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com
7	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2024-25	500	200	20
2025-26	500	200	20
2026-27	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
2	Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
3	Showing Practical Demonstrations to the learners	Through Virtual Simulation Software (Proteus- VSM) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
4	Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Simulation Software (Proteus- VSM) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
5	Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
6	Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Simulated Platform	Either 100% online in a virtual environment Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. Description:

This Standalone NOS provides a comprehensive overview of Static Timing Analysis (STA) in VLSI design, covering timing analysis fundamentals, including races, hazards, and setup and hold timing in both combinational and sequential circuits. Practical examples of setup and hold time violations and solutions are explored, alongside timing constraints for synthesis and circuit synthesis techniques. Advanced topics include timing performance improvement strategies such as pipelining and retiming, clock skew management, and open and closed-loop timing methodologies, with a focus on both block and chip level timing analysis. Students gain hands-on experience in Static Timing Analysis (STA) using Electronic Design Automation (EDA) tools, including timing analysis post-synthesis and place-and-route, interpretation of timing reports, Engineering Change Order (ECO) flows, and timing closure to meet sign-off requirements.

2. Scope:

The scope covers the following:

- Gain insight into timing analysis principles for combinational and sequential circuits, including races, hazards, and setup/hold timing, with practical examples illustrating setup/hold time violations and their resolutions.
- Acquire knowledge of timing constraints essential for synthesis and circuit synthesis techniques, establishing a strong foundation in timing analysis fundamentals.
- Explore advanced timing performance enhancement techniques such as pipeline, retiming, and clock skew management, addressing timing analysis at both block and chip levels.
- Gain hands-on experience in Static Timing Analysis (STA) using Electronic Design Automation (EDA) tools, covering post-synthesis, place-and-route timing analysis, timing report interpretation, ECO flows execution, and achieving timing closure, ensuring practical proficiency in applying STA methodologies in real-world VLSI design projects.

3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

Overview of VLSI STA:

PC1. Gain proficiency in Static Timing Analysis (STA) for VLSI design, encompassing analysis of timing in combinational and sequential circuits, resolution of timing issues like races and setup/hold violations through practical examples, and the establishment of synthesis-compatible timing constraints during circuit synthesis.

Timing performance:

PC2. Apply advanced techniques in timing performance enhancement, such as pipelining, retiming, and mitigation of clock skew issues, while conducting comprehensive timing analysis at block and chip levels to optimize design integrity and operational frequency across open and closed loop timing scenarios.

STA using EDA tools:

PC3. Utilize Electronic Design Automation (EDA) tools to apply Static Timing Analysis (STA), ensuring thorough timing analysis post synthesis and place-and-route stages to validate design timing constraints. Evaluate timing reports, manage Engineering Change Orders (ECO) flows, and conduct sign-off checks to achieve timing closure.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Develop a comprehensive understanding of timing analysis principles, encompassing races, hazards, setup and hold timing, and maximum frequency of operation for both combinational and sequential circuits.
- Recognize the importance of timing constraints in the synthesis process, gaining insight into circuit synthesis methodologies with a specific focus on timing analysis.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1. Ability to analyze complex timing issues in VLSI design, such as races, hazards, and setup/hold time violations, and devise effective solutions and Capacity to identify timing constraints and challenges during circuit synthesis and timing analysis, and apply analytical thinking to address them.

GS2. Proficiency in using Electronic Design Automation (EDA) tools for Static Timing Analysis (STA), including post-synthesis and place-and-route timing analysis, and interpreting timing reports.

GS3. Competence in executing Engineering Change Order (ECO) flows, conducting timing closure, and performing sign-off checks, demonstrating technical proficiency in utilizing EDA tools for VLSI design

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module Name	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project /Presentation/ Assignment Marks	Viva/ Internal Assessment (Marks)
Essentials of VLSI Circuits Timing Analysis **NOS Code: NIE/ELE/N0115**	**Overview of VLSI STA**	**30**	**20**	**-**	**6**
	Gain proficiency in Static Timing Analysis (STA) for VLSI design, encompassing analysis of timing in combinational and sequential circuits, resolution of timing issues like races and setup/hold violations through practical examples, and the establishment of synthesis-compatible timing constraints during circuit synthesis.	-	-	-	-
	Timing performance	**30**	**20**	**-**	**6**
	Apply advanced techniques in timing performance enhancement, such as pipelining, retiming, and mitigation of clock skew issues, while conducting comprehensive timing analysis at block and chip levels to optimize design integrity and operational frequency across open and closed loop timing scenarios.	-	-	-	-
	STA using EDA tools	**40**	**20**	**-**	**7**
	Utilize Electronic Design Automation (EDA) tools to apply Static Timing Analysis (STA), ensuring thorough timing analysis post synthesis and place-and-route stages to validate design timing constraints. Evaluate timing reports, manage Engineering Change Orders (ECO) flows, and conduct sign-off checks to achieve timing closure.	-	-	-	-
Total Marks -200		**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.