QUALIFICATION FILE – Standalone NOS

Essentials of RTL Coding for Synthesis

☐ Horizontal/Generic ☐ Vertical/Specialization

☒Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☐General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☒ Future Skills ☒ OEM

NCrF/NSQF Level: 4

Submitted By:

NATIONAL INSTITUTE OF ELECTRONICS AND INFORMATION TECHNOLOGY

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<tr><td>2.</td><td>Sector/s</td><td colspan="2">Electronics</td></tr>
<tr><td>3.</td><td>Type of Qualification ☒ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: NA</td><td>Qualification Name of the existing/previous version: NA</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version (Will be issued after NSQC approval.)</td><td>NG-04-EH-02902-2024-V1-NIELIT</td><td>5. NCrF/NSQF Level: 4</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">This standalone NOS in Essentials of RTL Coding for Synthesis aims to equip students with essential skills in VLSI design and IP development. It begins with an introduction to VLSI technology and design flow, emphasizing the importance of Register Transfer Level (RTL) design methodology. Students learn Verilog programming syntax, levels of abstraction, and test bench simulation techniques to design and develop IPs effectively. Practical sessions cover the implementation, emulation, debugging, and characterization of reusable IPs, ensuring comprehensive proficiency in Verilog RTL coding and synthesis for VLSI applications.</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
<table>
<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Relevant Experience (with Specialization - if applicable)</th></tr>
<tr><td>1</td><td>12th or equivalent in Science with Physics and Maths</td><td>NA</td></tr>
<tr><td>2</td><td>2 Years of 3-Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches after class 10th</td><td>NA</td></tr>
<tr><td>3</td><td>NSQF Level 3.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches</td><td>1.5 Years</td></tr>
</table></td></tr>
</table>

4	NSQF Level 3 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches	1.5 Years

b. Age: 18 Years

8.	**Credits Assigned to this NOS-Qualification, Subject to Assessment** *(as per National Credit Framework (NCrF))*	2 Credits	**9. Common Cost Norm Category (I/II/III)** *(wherever applicable)***:** Category-I
10.	**Any Licensing Requirements for Undertaking Training on This Qualification** *(wherever applicable)*	NA	
11.	**Training Duration by Modes of Training Delivery** *(Specify **Total Duration** as per selected training delivery modes and as per requirement of the qualification)*	☒ **Offline Only** ☐ **Online Only** ☐ **Blended**	

Training Delivery Mode	Theory (Hours)	Practical (Hours)	Total (Hours)
Classroom (offline)	**30**	**30**	**60**

The mode of delivery shall be based on the regional demand and can be offered in any of the above modes mentioned.

(Refer Blended Learning Annexure-V for details)

12. Assessment Criteria

Theory (Marks)	Practical (Marks)	Project/ Presentation /Assignment (Marks)	Viva/ Internal Assessment (Marks)	Total (Marks)	Passing %age
100	**60**	**20**	**20**	**200**	**50**

The centralised online assessment is conducted by the Examination Wing, NIELIT Headquarters.

13.	**Is the NOS Amenable to Persons with Disability**	☒ **Yes** ☐ **No If "Yes", specify applicable type of Disability:** **a.** Locomotor Disability: Leprosy Cured Person, Dwarfism, Muscular Dystrophy and Acid Attack Victims **b.** Visual Impairment: Low Vision	
14.	**Progression Path After Attaining the Qualification, wherever applicable** *(Please show Professional and Academic progression)*	*Design/Application Engineer/Team Lead / Project Manager*	
15.	**How participation of women will be encouraged?**	Participation by women can be ensured through Government Schemes. Occasionally, exclusive batches for women would be run for the proposed courses. Funding is available for women's participation under other schemes launched by the Government from time to time.	
16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	Qualification files available in English & Hindi Language.	
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	☐ **Yes** ☒ **No URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	**Name:** Jayaraj U Kidav **Email:** jayaraj@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Ishant Kumar Bajpai **Email:** ishant@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Deepam Dubey **Email:** deepamdubey@nielit.gov.in **Website:** https://nielit.gov.in/ **Name:** Sreejeesh S.G **Email:** sreejeesh@nielit.gov.in **Website:** https://nielit.gov.in/	
19.	**Final Approval Date by NSQC: 25.07.2024**	**20. Validity Duration: 3 Years**	**21. Next Review Date: 25.07.2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 2 year of experience in the field of VLSI Design
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	B.E./B. Tech in Electronics/ Electronics & Communication/ Electrical/ Electrical and Electronics/Instrumentation/ Electronics & Instrumentation / Instrumentation & Control /Computer Science/Information Technology Minimum 3 years of experience in the field of VLSI Design
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No *(If "Yes", details to be provided in Annexure)*
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NIL

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	B.Tech or Equivalent as per NCrF + 3 years relevant experience
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	The assessor carries out theory online assessments through the remote proctoring methodology. Theory examination would be conducted online and the paper comprises MCQ. Conduct of assessment is through trained proctors. Once the test begins, remote proctors have full access to the candidate's video feeds and computer screens. Proctors authenticate the candidate based on registration details, pre-test image captured and I-card in possession of the candidate. Proctors can chat with candidates or give warnings to candidates. Proctors can also take screenshots, terminate a specific user's test session, or re-authenticate candidates based on video feeds
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	External Examiners/ Observers (Subject matter experts) are deployed including NIELIT scientific officers who are subject experts for evaluation of Practical examination/ internal assessment / Project/ Presentation/ assignment and Major Project (if applicable). Qualification is generally B.Tech
4.	**Assessment Mode** *(Specify the assessment mode)*	Online for Theory Online/ Offline/ Blended for other assessment components depending on the region where the assessment is conducted

5.	**Tools and Equipment Required for Assessment**	☒ Same as for training ☐ Yes ☐ No *(details to be provided in Annexure-if it is different for Assessment)*

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No): Yes, Available at Annexure-A: Evidence of Need
2.	Number of Industry validations provided: 7
3.	Estimated number of people to be trained: 500 persons per year shall be trained.
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): NIELIT is recognized as AB and AA under Government Category. NIELIT is an HRD arm of MeitY, therefore, the Line Ministry Concurrence is not required.
5.	Latest Skill Gap Study (not older than 2 years) (Yes/No): Yes, Available in Annexure-A: Evidence of Need
6.	Latest Market Research Reports or any other source (not older than 2 years) (Yes/No): Yes, Available at Annexure-A: Evidence of Need

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	*Available at* Annexure-I: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	*Available at* Annexure-II: Tools and Equipment
3.	**Annexure: Industry Validation**	*Available at* Annexure-III: Industry Validation
4.	**Annexure: Training Details**	*Available at* Annexure-IV: Training Details
5.	**Annexure:** Blended Learning *(Mandatory, in case the selected Mode of delivery is Blended Learning)*	*Available at* Annexure-V: Blended Learning

6.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	*Available at* Annexure-VI: Standalone NOS- Performance Criteria details
7.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	*Available at* Annexure-VII: Detailed Assessment Criteria
8.	**Annexure:** Assessment Strategy *(Mandatory)*	*Available at* Annexure-VIII: Assessment Strategy
9.	**Annexure:** Acronym and Glossary *(Optional)*	*Available at* Annexure-IX: Acronym and Glossary
10.	**Supporting Document:** Model Curriculum	*Available at* Annexure-C: Model Curriculum

Annexure- I: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	• Gain a thorough grasp of VLSI technology, encompassing its applications and the entire design flow, alongside proficiency in Register Transfer Level (RTL) design fundamentals, methodology, and the use of Hardware Description Languages (HDLs) such as Verilog or VHDL • Develop expertise in both combinational and sequential logic design principles, covering Boolean algebra, logic gates, flip-flops, registers, and state machines. Master the use of Verilog and other HDLs to efficiently design combinational and sequential logic circuits, and adeptly write RTL code for basic digital circuit implementations. • Expertise in functional verification techniques for RTL designs, including the development of test benches and the simulation and debugging of RTL designs.	• Possesses specialized knowledge in VLSI technology and RTL design, demonstrating proficiency in digital circuit principles and their applications in hardware description languages. • Applies theoretical knowledge effectively to ensure the quality and timing accuracy of digital circuits.	**4**
Professional and Technical Skills/ Expertise/ Professional	• Master the basics of Register Transfer Level (RTL) design, including understanding its methodology and process. • Acquire comprehensive knowledge of combinational and	• Demonstrates technical proficiency in RTL design, utilizing HDLs for complex digital designs	**4**

Knowledge	sequential logic design concepts, encompassing Boolean algebra, logic gates, flip-flops, registers, and state machines. • Implement functional verification techniques for RTL designs, including the development and utilization of test benches for thorough testing.	and testing for functional accuracy. • Uses systematic approaches to verify design functions, interpreting data accurately for high-quality output.	
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	• Acquire a solid understanding of VLSI technology and its applications, along with mastery of the VLSI design flow. • Develop expertise in RTL design methodology, encompassing basics, process overview, and methodology, and effectively utilize HDLs like Verilog or VHDL for design implementation. • Gain proficiency in digital logic design principles, including combinational and sequential logic concepts, Boolean algebra, logic gates, and the implementation of flip-flops, registers, and state machines.	• Demonstrates an entrepreneurial mindset in digital design, understanding key processes to deliver optimized solutions. • Possesses proficient technical skills in design flow and HDL usage, promoting readiness for the professional landscape.	**4**
Broad Learning Outcomes/Core Skill	• Gain comprehensive expertise in VLSI design, encompassing a deep understanding of VLSI technology and its applications, proficiency in RTL design methodology using HDLs like Verilog or VHDL, and practical skills in digital logic design, RTL simulation, verification, timing analysis, and resolution of setup and hold time violations.	• Demonstrates logical reasoning and technical skills necessary for the effective design and verification of digital circuits. • Core knowledge in timing analysis and issue resolution strengthens reliability in various design scenarios.	**4**
Responsibility	• Ability to manage the system resources most effectively by appropriate planning, estimation, coordination and control of the activities involved in the design & development of any task/project	• Takes complete responsibility for delivery and quality of own work and output as also the subordinates. • Shares responsibility for the group tasks.	**4**

Annexure-II: Tools and Equipment (lab set-up)

List of Tools and Equipment

Batch Size: 30

Description		Qty	Specifications
1	Classroom	1	30 Sq.m
2	Student Chair	30	
3	Student Table	30	
4	LCD Projector	1	
5	Trainer Chair & Table	1	
6	Pin up Boards	1	
7	White Board	1	
	VLSI Design Lab		60 Sq. m
1	Desktop computer with accessories	30	Processor: Intel Core i5 (sixth generation newer) or equivalent Memory: 16GB RAM, Internal Storage: 500GB Xilinx Zynq Series FPGAs
2	Desk jet printer	1	A4
3	CADENCE/Synopsys frontend and backend university bundle	5 user licenses	Server-based floating licenses.
4	Xilinx Vivado design suite	30 user licenses	Server-based floating licenses.

Classroom Aids
The aids required to conduct sessions in the classroom are:

1. LCD Projector/Smart Board

Annexure-III: Industry Validations Summary

S. No	Organization Name	Representative Name	Designation	Contact Address	Contact Phone No	E-mail ID
1	B. G. Infotech	Amal Das	Centre Head	Kakdihi, Mecheda, Purba, Medinipur	9434996748	bginfotech2007@gmail.com
2	Inditech Software Wizard Pvt. Ltd.	Sandip Ghosh	Course Coordinator	Mohiari Chanpiritala, Po: Andul Mouri, PS: Domjur, Distt: Howrah, West Bengal-711302	9230027415	swizardrecruitment@gmail.com
3	Aajivika Global Skill Private Limited	Mukesh Kumar Verma	Director	Beside Vishal Trade, dasmile chowk, Khunti Road Ranchi, Jharkhand-835221	9507952882	aajivikaglobal@gmail.com
4	AISECT Ltd.	Teena Panthi	Assistant Manager	AISECT Ltd. 1-1-387, 3rd floor, Flat No. 403/404, GNR Heights, Above SBI,Bakaram Road, Musheerabad, Hydrabad-500020	7879982075	teena.panthi@aisect.org
5	Surekha IT Services	Anjani K	Manager	8-3-191/84/302, Sharan Residency, Vengalrao Nagar, Hyderabad-500038, Telangana	8125134134	info@surekhaitservices.com
6	Prasanthi Polytechnic	D. Prasad	Principal	Duppituru (Vill), Atchutapuram (Md). Visakhapatnam (Dist), Andhara Pradesh-531011	9849952573	prasadreddy.1279@gmail.com
7	Sidhi Vinayak Academy	Neha Verma	Director	Shiv Narayan Kunj, B Block, Shivaji Nagar, Hethu, Ranchi, JH-834002	8789837772	sidhiacadmey@gmail.com

Annexure-IV: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability
2024-25	500	200	20
2025-26	500	200	20
2026-27	1000	200	20

Data to be provided year-wise for next 3 years.

Annexure-V: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

S. No.	Select the Components of the Qualification	List Recommended Tools – for all Selected Components	Offline : Online Ratio
1	Theory/ Lectures - Imparting theoretical and conceptual knowledge	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
2	Imparting Soft Skills, Life Skills, and Employability Skills /Mentorship to Learners	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
3	Showing Practical Demonstrations to the learners	Through Virtual Simulation Software (Proteus- VSM) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
4	Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Through Virtual Simulation Software (Proteus- VSM) and Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
5	Tutorials/ Assignments/ Drill/ Practice	Online interaction platforms like JitSi Meet, Bharat VC, Google Meet, MS Teams, etc.	70:30
6	Proctored Monitoring/ Assessment/ Evaluation/ Examinations	NIELIT Remote Proctored Software	Online: 100% Theory Offline: 100% Practical
7	On the Job Training (OJT)/ Project Work Internship/ Apprenticeship Training	Simulated Platform	Either 100% online in a virtual environment

			Or 100% offline in the Industry.

Annexure-VI: Standalone NOS- Performance Criteria details

1. Description:

The standalone NOS provides foundational skills in VLSI design, focusing on RTL coding using Verilog. This module introduces students to the VLSI design cycle, RTL design methodology, and essential digital logic principles, including combinational and sequential logic. Through practical sessions, students learn Verilog syntax, develop RTL code, and gain experience with functional verification techniques, test bench simulation, and debugging. The module also covers timing constraints and analysis, preparing students to optimize and resolve timing issues, enabling them to design efficient, reusable IPs for VLSI applications.

2. Scope:

The scope covers the following:

Gain a comprehensive understanding of VLSI technology, its significance, and applications, providing a solid foundation for further learning and understand the complete VLSI design flow, including the basics of Register Transfer Level (RTL) design, its process, and methodology.

3. Elements and Performance Criteria

To be competent, the user/individual on the job must be able to:

PC1. RTL Design Methodology

- Understand the basics of Register Transfer Level (RTL) design.
- Demonstrate proficiency in the RTL design process and methodology.

PC2. Digital Logic Design Principles

- Apply combinational and sequential logic design concepts effectively.
- Utilize Boolean algebra and logic gates to design digital circuits.

PC3. RTL Design Using HDL

- Demonstrate proficiency in Verilog syntax and constructs.
- Design combinational and sequential logic circuits using HDL.

PC4. RTL Simulation and Verification

- Develop and utilize test benches for comprehensive testing.
- Perform simulation and debugging of RTL designs to ensure functionality and correctness.

4. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

- Grasping the essence of VLSI technology and its versatile applications across industries. Acquiring knowledge about the complete VLSI design flow, from conceptualization to fabrication, and its significance.
- Developing a solid understanding of digital logic principles, including combinational and sequential logic.
- Acquiring skills in functional verification techniques, test bench development, and timing analysis essential for robust RTL designs.

5. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1. Developing problem-solving skills and analytical thinking to tackle complex RTL design challenges effectively.

GS2. Enhancing communication skills for effectively conveying design ideas and collaborating with team members on RTL design projects.

GS3. Cultivating attention to detail to ensure accuracy in RTL design, simulation, and verification, while also adapting to changing design requirements and methodologies.

Annexure-VII: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

NOS/Module Name	Assessment Criteria for Performance Criteria	Theory Marks	Practical Marks	Project /Presentation/ Assignment Marks	Viva/ Internal Assessment (Marks)
NOS1: Essentials of RTL Coding for Synthesis **NOS Code: NIE/ELE/N0114**	**RTL Design Methodology**	25	15	-	5
	Understand the basics of Register Transfer Level (RTL) design.	-	-	-	-
	Demonstrate proficiency in the RTL design process and methodology.	-	-	-	-
	Digital Logic Design Principles	25	15	-	5
	Apply combinational and sequential logic design concepts effectively.	-	-	-	-
	Utilize Boolean algebra and logic gates to design digital circuits.	-	-	-	-
	RTL Design Using HDL	25	15	-	5
	Demonstrate proficiency in Verilog syntax and constructs	-	-	-	-
	Design combinational and sequential logic circuits using HDL.	-	-	-	-
	RTL Simulation and Verification	25	15	-	5
	Develop and utilize test benches for comprehensive testing.	-	-	-	-
	Perform simulation and debugging of RTL designs to ensure functionality and correctness.	-	-	-	-
Total Marks -200		**100**	**60**	**20**	**20**

Annexure-VIII: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

Assessment of the qualification evaluates candidates to ascertain that they can integrate knowledge, skills and values for carrying out relevant tasks as per the defined learning outcomes and assessment criteria.

The underlying principle of assessment is fairness and transparency. The evidence of the outcomes and assessment criteria. competence acquired by the candidate can be obtained by conducting Theory (Online) examination.

About Examination Pattern:

1. The question papers for the theory exams are set by the Examination wing (assessor) of NIELIT HQS.

2. The assessor assigns roll number.

3. The assessor carries out theory online assessments. Theory examination would be conducted online and the paper comprise of MCQ

4. Pass percentage would be 50% marks.

5. The examination will be conducted in English language only.

Quality assurance activities: A pool of questions is created by a subject matter expert and moderated by other SME. Test rules are set beforehand. Random set of questions which are according to syllabus appears which may differ from candidate to candidate. Confidentiality and impartiality are maintained during all the examination and evaluation processes.

Annexure-IX: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A grouping of professional activities on the basis of their main economic function, product, service or technology.