QUALIFICATION FILE – Standalone NOS

Essentials of VLSI Design

☒ Horizontal/Generic ☒ Vertical/Specialization

☒ Upskilling ☐ Dual/Flexi Qualification ☐ For ToT ☐ For ToA

☒General ☐ Multi-skill (MS) ☐ Cross Sectoral (CS) ☐ Future Skills

NCrF/NSQF Level: 5.0

NOS ID: HCLT/N0046/IT/2024

Submitted By:

HCL Technologies Ltd.

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Section 1: Basic Details

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<tr><td>3.</td><td>Type of Qualification ☐ New ☐ Revised</td><td>NQR Code & version of the existing /previous qualification: (change to previous, once approved)</td><td>Qualification Name of the existing/previous version: (previous, once approved)</td></tr>
<tr><td>4.</td><td>National Qualification Register (NQR) Code & Version (Will be issued after NSQC approval.)</td><td>NG-05-IT-02989-2024-V1-HCL</td><td>5. NCrF/NSQF Level:5.0</td></tr>
<tr><td>6.</td><td>Brief Description of the Standalone NOS</td><td colspan="2">As a VLSI design engineer one must develop algorithms and methodologies for optimizing VLSI designs, collaborate with cross-functional teams to enhance VLSI performance and efficiency</td></tr>
<tr><td>7.</td><td>Eligibility Criteria for Entry for a Student/Trainee/Learner/Employee</td><td colspan="2">a. Entry Qualification & Relevant Experience:
<table>
<tr><th>S. No.</th><th>Academic/Skill Qualification (with Specialization - if applicable)</th><th>Relevant Experience (with Specialization - if applicable)</th></tr>
<tr><td>1.</td><td>Completed 2nd year of UG in relevant field*
(OR)
Pursuing 2nd year of UG and continuing education
*Relevant field - IT/ Computer Science, Electrical & Electronics streams.</td><td>.</td></tr>
</table>
b. Age: NA</td></tr>
<tr><td>8.</td><td>Credits Assigned to this NOS-Qualification, Subject to Assessment (as per National Credit Framework (NCrF))</td><td>7 Credits</td><td>9. Common Cost Norm Category (I/II/III) (wherever applicable):I</td></tr>
</table>

<table>
<tr><td>10.</td><td>Any Licensing Requirements for Undertaking Training on This Qualification (wherever applicable)</td><td>No</td></tr>
<tr><td>11.</td><td>Training Duration by Modes of Training Delivery (Specify Total Duration as per selected training delivery modes and as per requirement of the qualification)</td><td>☐ Offline Only ☐ Online Only ☒ Blended
<table><tr><th>Training Delivery Mode</th><th>Theory (Hours)</th><th>Practical (Hours)</th><th>Total (Hours)</th></tr><tr><td>Blended (Virtual Classrooms)</td><td>90</td><td>120</td><td>210</td></tr><tr><td>Online</td><td></td><td></td><td></td></tr></table>(Refer Blended Learning Annexure for details)</td></tr>
<tr><td>12.</td><td>Assessment Criteria</td><td><table><tr><th>Theory (Marks)</th><th>Practical (Marks)</th><th>Project (Marks)</th><th>Viva (Marks)</th><th>Total (Marks)</th><th>Passing %age</th></tr><tr><td>50</td><td>100</td><td>50</td><td>0</td><td>200</td><td>70</td></tr></table><u>Assessments are administered through one of the following methods.</u>
Daily Quiz (FA) - Online
Assignments (FA) - Offline
Multi Choice Questions (SA) – Online<ol type="a">
Consists of Easy, Medium and Hard Questions also consisting of Scenario Based Questions.
Projects (SA) – Offline
Industry Use Case Scenarios will be provided as Problem Statements in the Platform for which,
the Projects need to be Developed, Tested and Submitted for Evaluation.
Lab Assessment (SA) - Practical Hands-On for Industry Aligned Project Scenarios.</td></tr>
<tr><td>13.</td><td>Is the NOS Amenable to Persons with Disability</td><td>☐ Yes ☒ No If “Yes”, specify applicable type of Disability:</td></tr>
<tr><td>14.</td><td>Progression Path After Attaining the Qualification, wherever applicable (Please show Professional and Academic progression)</td><td>NA</td></tr>
</table>

15.	**How participation of women will be encouraged?**	Almost all companies today have signed up improving gender diversity, as well as recruit women from rural India (ESG compliance). We believe that the industry relevant programs can build more confidence in women to apply to multi-national companies. The program has been designed to encourage candidates even from non-Engineering/non-Science backgrounds to embrace tech careers. Given the fact that globally including India, women participation in STEM careers is below 20%, we believe only such skilling programs can encourage gender diversity.	
16.	**Other Indian languages in which the Qualification & Model Curriculum are being submitted**	*(Please provide assurance and plan for developing the qualification in other Indian Languages as per training requirement))*	
17.	**Is similar NOS available on NQR-if yes, justification for this qualification**	☐ **Yes** ☐ **No** **URLs of similar Qualifications:**	
18.	**Name and Contact Details Submitting / Awarding Body SPOC** *(In case of CS or MS, provide details of both Lead AB & Supporting ABs)*	**Name:** Shanthi Venkatraman **Designation:** Global Lead - Customer Assurance **Email:** shanthi.venkatraman@hcl.com **Contact No.: +91 9600122611** **Website:** https://www.hcltech.com/	
19.	**Final Approval Date by NSQC: 27 Aug 2024**	**20. Validity Duration:3 Years**	**21. Next Review Date: 27 Aug 2027**

Section 2: Training Related

1.	**Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	Graduation with min. of 5 years' experience in VLSI Design or its equivalent
2.	**Master Trainer's Qualification and experience in the relevant sector (in years)** *(as per NCVET guidelines)*	Graduation with min. of 7 years' experience in VLSI Design or its equivalent
3.	**Tools and Equipment Required for the Training**	☒Yes ☐No *(If "Yes", details to be provided in Annexure)*
4.	**In Case of Revised NOS, details of Any Upskilling Required for Trainer**	NA

Section 3: Assessment Related

1.	**Assessor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	Graduation (in EEE/ECE) with a minimum of 5 years' experience in VLSI design or its equivalent.
2.	**Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines), (wherever applicable)*	Graduation (in EEE/ECE) with a minimum of 5 years' experience in VLSI design or its equivalent.
3.	**Lead Assessor's/Proctor's Qualification and experience in relevant sector (in years)** *(as per NCVET guidelines)*	Graduation (in EEE/ECE) with min. of 7 years of experience in VLSI design or its equivalent.
4.	**Assessment Mode** *(Specify the assessment mode)*	Online / Proctored / AI Proctored
5.	**Tools and Equipment Required for Assessment**	☒ Same as for training ☐ Yes ☐ No *(details to be provided in Annexure-if it is different for Assessment)*

Section 4: Evidence of the Need for the Standalone NOS

Provide Annexure/Supporting documents name.

1.	Government /Industry initiatives/ requirement (Yes/No):
2.	Number of Industry validation provided: NA
3.	Estimated number of people to be trained: Approx. 15,000 learners to be trained in the year 2024
4.	Evidence of Concurrence/Consultation with Line/State Departments (In case of regulated sectors): (Yes/No): Yes, HCLTech has been working to employ local candidates from diverse backgrounds in Tier 2 towns like Madurai, Vijayawada, and Lucknow as part of an agreement with State Governments. We have been using this Embedded IoT developer AI QP for skilling and employment. If "No", why: NA

Section 5: Annexure & Supporting Documents Check List

Specify Annexure Name / Supporting document file name

1.	**Annexure:** NCrF/NSQF level justification based on NCrF/NSQF descriptors *(Mandatory)*	Annexure: Evidence of Level
2.	**Annexure:** List of tools and equipment relevant for NOS *(Mandatory, except in case of online course)*	Annexure: Tools and Equipment
3.	**Annexure:** Performance and Assessment Criteria *(Mandatory)*	Annexure: Performance and Assessment Criteria
4.	**Annexure:** Assessment Strategy *(Mandatory)*	Annexure: Assessment Strategy
5.	**Annexure:** Blended Learning *(Mandatory, in case selected Mode of delivery is Blended Learning)*	Annexure: Blended Learning
6.	**Annexure:** Acronym and Glossary *(Optional)*	Annexure: Acronym and Glossary
7.	**Annexure/Supporting Document:** Standalone NOS-Performance Criteria Details Annexure/Document with PC-wise detailing as per NOS format (Mandatory- Public view)	Annexure: Standalone NOS Performance Criteria
8.	**Supporting Document:** Model Curriculum *(Mandatory – Public view)*	Model Curriculum – Essentials of VLSI Design

Annexure: Evidence of Level

NCrF/NSQF Level Descriptors	Key requirements of the job role/ outcome of the qualification	How the job role/ outcomes relate to the NCrF/NSQF level descriptor	NCrF/NSQF Level
Professional Theoretical Knowledge/Process	1. Understanding of VLSI Design Principles: Gain a comprehensive understanding of VLSI design principles, including semiconductor physics, CMOS technology, circuit design basics, and advanced digital design techniques, to develop a solid foundation for designing integrated circuits. 2. Optimization and Performance Analysis: Develop skills in optimizing VLSI designs for different applications, focusing on performance metrics such as speed, power efficiency, and area utilization. Learn techniques for analyzing and improving performance. 3. Testing, Verification, and Validation: Understand the importance of testing, verification, and validation in VLSI design. Learn methods for ensuring correctness, including fault modeling, design for testability (DFT) techniques, and post-silicon validation strategies.	1. Understanding of Advanced VLSI Principles: Students will demonstrate a comprehensive understanding of advanced VLSI design principles, including semiconductor physics, device modeling, circuit design, and layout techniques, enabling them to develop efficient and optimized VLSI systems. 2. Knowledge of Emerging Trends: Students will stay abreast of emerging trends in both VLSI design, demonstrating awareness of, research directions, and industry developments, and their implications for future VLSI. 3. Critical Analysis and Problem-Solving Skills: Students will develop critical thinking skills to analyze complex VLSI design challenges by identifying innovative solutions, evaluating trade-offs, and making informed design decisions to achieve optimal performance and efficiency.	5.0

Professional and Technical Skills/ Expertise/ Professional Knowledge	1.Master VLSI Design Fundamentals: Understand the principles of VLSI design, including semiconductor physics, device modeling, CMOS technology, digital and analog circuit design, timing analysis, and design methodologies, laying a strong foundation for advanced study and specialization. 2. Proficiency in CAD Tools and Methodologies: Gain proficiency in using EDA tools specific to VLSI design, including industry-standard tools for layout, simulation, synthesis, and verification, enabling efficient design, analysis, and validation of complex VLSI circuits and systems. 3. Advanced Knowledge in VLSI Testing and Verification: Acquire advanced knowledge in VLSI testing and verification techniques, including fault models, design for testability (DFT) methodologies, post-silicon validation, and debugging, ensuring the robustness and reliability of VLSI designs 4. Hands-on Experience in Project Implementation: Apply theoretical knowledge and practical skills acquired throughout the program to design, implement, and evaluate real-world	1. Proficient Design and Optimization Skills: Students will demonstrate proficiency in designing and optimizing VLSI circuits and systems. This includes understanding the trade-offs between performance, power consumption, area, and reliability. 2. Hands-On Experience with EDA Tools Students will acquire hands-on experience with industry-standard for VLSI design and simulation, as well as familiarity with FPGAs. They can effectively use these tools to design, simulate, synthesize, implement and verify. 3. Expertise in Low-Power Design Techniques. Students will develop expertise in low-power design techniques including voltage scaling, clock gating, power gating, and dynamic voltage and frequency scaling (DVFS). They will understand the impact of these techniques on power consumption, performance, and reliability and apply them to optimize the energy efficiency of VLSI designs.	5.0

	projects integrating VLSI design, addressing challenges such as power optimization, performance enhancement, and hardware-software co-design. 5. Stay Updated with Emerging Technologies: Stay abreast of the latest advancements and emerging trends in VLSI design and related fields through continuous learning, professional development activities, and engagement with industry forums, conferences, and research publications, fostering a culture of lifelong learning and innovation.	4. Proficiency in Testing, Verification, and Post-Silicon Validation: Students will demonstrate proficiency in testing, verification, and post-silicon validation of VLSI designs applications. They will understand the importance of design for testability (DFT) techniques, fault modeling, and simulation-based verification methods in ensuring correctness and reliability. 5. Ability to Innovate and Adapt to Emerging Technologies: Students will develop the ability to innovate and adapt to emerging technologies and trends in VLSI design They will be equipped with the knowledge and skills to stay updated with the latest advancements in both fields and apply them to solve real-world problems, driving innovations in advanced and mixed VLSI design.	
Employment Readiness & Entrepreneurship Skills & Mind-set/Professional Skill	1. Understanding Industry Trends: Develop the ability to analyze and comprehend current and emerging trends in the VLSI industries. Identify opportunities and challenges presented by advancements in	1.Proficiency in Integrated Circuit (IC) Design Students will demonstrate proficiency in VLSI design principles and techniques, including IC fabrication processes, circuit design, and layout. Additionally, they will integrate concepts and algorithms	5.0

	technology, market demands, and regulatory landscapes. 2. Entrepreneurial Mindset Cultivation: Foster an entrepreneurial mindset by encouraging creativity, innovation, and risk-taking in VLSI design applications. Cultivate the skills to identify, evaluate, and pursue entrepreneurial opportunities in the VLSI sectors. 3. Professional Communication and Networking: Enhance communication skills to effectively convey technical ideas, project proposals, and business plans to diverse stakeholders. Develop networking skills to build professional relationships within the VLSI communities, fostering collaboration and partnership opportunities. 4. Project Management and Leadership: Acquire project management skills to plan, execute, and deliver VLSI design projects with integration on time and within budget. Develop leadership qualities to inspire and motivate teams, drive innovation, and navigate challenges in VLSI.	into VLSI designs to develop innovative solutions. 2. Problem-solving and Innovation Abilities: Students will develop strong problem-solving skills and demonstrate the ability to innovate in the field of VLSI design. They will apply critical thinking and creativity to address complex engineering challenges, identify opportunities for improvement, and propose novel solutions. 3. Entrepreneurial Mind-set and Business Acumen: Students will cultivate an entrepreneurial mindset and understand business fundamentals relevant to the VLSI design industry. They will learn to identify market opportunities, assess the commercial viability of their designs, and develop business plans for potential entrepreneurial ventures or product commercialization. 4. Effective Communication and Collaboration Skills: Students will enhance their communication and collaboration skills, both within multidisciplinary engineering teams	

	5.Ethical and Social Responsibility: Understand the ethical implications of VLSI design applications, including issues related to privacy, bias, and fairness. Cultivate a sense of social responsibility by exploring ways to leverage VLSI technologies for positive societal impact while mitigating potential risks. 6.Career Development and Adaptability: Develop strategies for continuous learning and skill enhancement to stay updated with evolving VLSI and AI technologies and methodologies. Enhance adaptability to navigate dynamic career paths, including opportunities in traditional employment, freelance consulting, entrepreneurship, and academia.	and with stakeholders from diverse backgrounds. They will effectively convey technical concepts, present their ideas persuasively, and work collaboratively to achieve project goals. 5. Adaptability to Emerging Technologies and Market Trends: Students will demonstrate adaptability to emerging technologies and market trends in the rapidly evolving fields of VLSI design. They will stay updated on the latest advancements, industry standards, and regulatory requirements, and continuously refine their skills to remain competitive in the job market or entrepreneurial landscape. 6. Ethical and Professional Conduct: Students will uphold ethical and professional standards in their practice as VLSI design engineers with expertise. They will demonstrate integrity, accountability, and respect for intellectual property rights, while adhering to relevant legal and ethical guidelines governing the design,	

		development, and deployment of VLSI-based solutions.	
Responsibility	1.. Ensuring Design Efficiency and Performance: Analyze the performance metrics relevant VLSI designs, such as power consumption, speed, and area utilization. Apply optimization techniques to enhance the efficiency and performance of VLSI designs. Assess trade-offs between design complexity, resource utilization, and performance requirements in VLSI systems. 3. Addressing Ethical and Security Considerations: Identify ethical implications associated with VLSI designs, including privacy concerns, bias mitigation, and algorithmic transparency. Implement security measures to safeguard VLSI design against potential threats such as tampering, reverse engineering, and malicious attacks. Evaluate legal and regulatory frameworks governing the responsible deployment of VLSI systems,	1. Ethical Awareness: Upon completion of the course, students should understand the ethical considerations inherent in designing VLSI circuits. This includes recognizing potential biases in VLSI, understanding the implications of technologies and adhering to ethical standards in the development. 2. Risk Management: Students should be able to identify and assess potential risks associated with VLSI design, such as reliability issues, security vulnerabilities, and unintended consequences. They should develop strategies for mitigating these risks through robust design practices, rigorous testing methodologies, and adherence to industry standards and regulations. 3. Sustainability: Upon completion of the course, students should appreciate the environmental impact of VLSI design technologies and be able to incorporate principles of sustainability into their design processes. This includes optimizing	5.0

	including compliance with industry standards and intellectual property rights. 4. Collaborating Across Disciplines for Holistic Solutions: Foster interdisciplinary collaboration between VLSI engineers, researchers, and domain experts to address complex design challenges and optimize system performance. Communicate effectively with stakeholders to articulate the benefits, limitations, and risks associated with VLSI designs. 4. Engage in continuous learning and professional development to stay abreast of emerging technologies, industry trends, and best practices in responsible VLSI design	power consumption in VLSI circuits, minimizing electronic waste through efficient design practices, and considering the lifecycle impacts of VLSI products on the environment. 4. Professional Integrity: Students should demonstrate a commitment to professional integrity and accountability in their roles as VLSI design engineers. This involves maintaining transparency and honesty in their work, upholding intellectual property rights and confidentiality agreements, and taking responsibility for the social and ethical implications of the technologies they help to develop. They should also engage in continuous learning and professional development to stay informed about emerging ethical issues and best practices in the field.	

Annexure: Tools and Equipment (lab set-up)

List of Tools and Equipment

Batch Size:

S. No.	Tool / Equipment Name	Specification	Quantity for specified Batch size
1.	Computer	I3/i5 with 16 GB RAM	One per learner
2.	Wokwi on- line simulator	https://wokwi.com/	Installed on the computer
3.	VLSI EDA Tools		Installed on the computer
4.	Cadence Virtuoso ADE	https://www.cadence.com/en_US/home/support/software-downloads.html	Installed on the computer
5.	EDA playground (Verilog code)	Online tool	
6.	Yosys(Verilog code)	Yosys Open SYnthesis Suite :: About (yosyshq.net)	
7.	XSchem(Schematic)	https://github.com/StefanSchippers/xschem.git xschem-src	
8.	NGSPICE(simulate netlist)	ngspice.sourceforge.io/download.html	
9.	Magic VLSI(layout)	opencircuitdesign,com/magic/download.html	
10.	NetGen(DRC, LVS)	opencircuitdesign.com/netgen	
11.	OpenTimer(Static Timing Analysis)	https://github.com/.OpenTimer/OpenTimer	GNU C++compiler v7.3 with –std=c++1z
12.	SkyWater Sky130PDK(130nm)	https://www.skywatertechnology.com/sky130-open-source-pdk/	

Classroom Aids

The aids required to conduct sessions in the classroom are:

1. Projector or MS Teams (for virtual) with Wi-Fi Connectivity
2. Computer system (1 per learner)

Annexure: Industry Validations Summary

Not Applicable - *vide Guidelines for Creditisation of Skilling and Training Courses and Qualifications of MNCs and Leading Indian Enterprises*

Annexure: Training Details

Training Projections:

Year	Estimated Training # of Total Candidates	Estimated training # of Women	Estimated training # of People with Disability

Data to be provided year-wise for next 3 years.

Annexure: Blended Learning

Blended Learning Estimated Ratio & Recommended Tools:

Refer NCVET "Guidelines for Blended Learning for Vocational Education, Training & Skilling" available on:
https://ncvet.gov.in/sites/default/files/Guidelines%20for%20Blended%20Learning%20for%20Vocational%20Education,%20Training%20&%20Skilling.pdf

S. No.	Select the Components of the NOS	List Recommended Tools – for all Selected Components	Offline: Online Ratio
1	☒Theory/ Lectures - Imparting theoretical and conceptual knowledge	Career Shaper platform	30:70
2	☒Imparting Soft Skills, Life Skills and Employability Skills /Mentorship to Learners	Career Shaper platform, MS Teams	10:90
3	☒Showing Practical Demonstrations to the learners	Code Lab / Assignments upload in LMS	0:100
4	☒Imparting Practical Hands-on Skills/ Lab Work/ workshop/ shop floor training	Code Lab / Assignments upload in LMS	0:100

5	☒Tutorials/ Assignments/ Drill/ Practice	Discussion Forum, P2P Chat Forums	0:100
6	☒Proctored Monitoring/ Assessment/ Evaluation/ Examinations	Online AI Proctored Assessment (Theory and Lab based)	0:100
7	☒On the Job Training (OJT)/ Project Work Internship/ Candidate Training	Industry domain-based Project	10:90

Annexure: Standalone NOS- Performance Criteria details

Scope:

The scope covers the following:

VLSI Front end: Generate netlist, simulate, Synthesis, get the netlist, generate report and analyze with design specification and constraints

1. Digital VLSI design: Verilog Program and Test bench with all test cases- Logic design, RTL design, Synthesis, FPGA example-10 projects

VLSI Back end:

2. Physical design: Schematic and Layout with DRC and LVS**,** Floor planning, Placement, Routing and Clock Tree Synthesis, STA-10 projects

3. Analog VLSI design: Schematic and Layout with DRC and LVS**,** Floor planning, Placement, Routing and Clock Tree Synthesis, Transient Analysis, DC Analysis and AC Analysis - 5 projects

4. Verification and Validation: Functional verification, Timing verification, Power verification, Formal verification - 5 projects

5. Test and Debug: Design for testability (front end), Post silicon validation: 2 projects

1. Elements and Performance Criteria

Fundamentals of VLSI Design & Semiconductors - 15 hours

Mapped to **: HCLT/N0046/IT/2024**

To be competent, the user/individual on the job must be able to:
PC1. Introduction of MOS Device Physics, CMOS technology, VLSI Life cycle.
PC2. Apply the required logic to provide a solution for the problems.

Getting Started with Digital Design & VLSI Representation– 15 Hours

Mapped to **: HCLT/N0046/IT/2024**

To be competent, the user/individual on the job must be able to:
PC3. Introduction to Digital design
PC4. Combinational ,Sequential logic design and State machines

Essentials of RTL Verilog Coding – 30 Hours

Mapped to **: HCLT/N0046/IT/2024**

To be competent, the user/individual on the job must be able to:
PC5. Introduction to Hardware Description Languages
PC6. Basics of RTL Design - Verilog
PC7. Datapath building blocks- Combinational Elements and Sequential Elements of RTL Design
PC8: Controller building blocks -State Machines
PC9: Memories
PC10: RTL Methodology and Timing

Getting Started with VLSI Design Flow Methodologies– 30 Hours

Mapped to: **HCLT/N0046/IT/2024**

To be competent, the user/individual on the job must be able to:

PC11: Steps in the physical design flow (RTL to GDSII) / ASIC design flow
PC12: Design methodologies: Full custom, Semi-custom, Standard cell/ FPGA
PC13: Design for manufacturability (DFM)

Getting Started with Logic Synthesis & Optimization Processes – 15 Hours

Mapped to **: HCLT/N0046/IT/2024**

To be competent, the user/individual on the job must be able to:
PC14: Objective of Logic Synthesis and Synthesis Flow
PC15: Function for Synthesis, Constraints on Synthesis and CTS
PC16: 2-level and multi-level optimization
PC17: Algebraic Model and Algebraic Model

Fundamentals of Low Power Design Techniques– 15 Hours

Mapped to **: HCLT/N0046/IT/2024**

To be competent, the user/individual on the job must be able to:
PC18: Sources of power dissipation: Dynamic and static power
PC19: Power estimation techniques, Power optimization strategies
PC20: Power Analysis (IR Drop)

Essentials of VLSI Physical Design– 30 Hours

Mapped to **: HCLT/N0046/IT/2024**

To be competent, the user/individual on the job must be able to:
PC21: Overview of the physical design flow, Comparison between frontend and backend
PC22: Circuit and Layout and IC fabrication
PC23: Floor Planning, Placement and Routing

Essentials of VLSI Testing & Verification Methodologies – 30 Hours

Mapped to **: HCLT/N0046/IT/2024**

To be competent, the user/individual on the job must be able to:

PC24: Functional verification techniques and Formal verification methods
PC25: Design for testability (DFT) and Testing methodologies and fault models. - Front end
PC26: Unified Verification Methodology (UVM)- Front end
PC27: Clock tree synthesis (CTS)
PC28: DRC, LVS and ERC- Backend
PC29: Static Timing Analysis (STA)

Industry aligned projects– 30 Hours
Mapped to **: HCLT/N0046/IT/2024**

To be competent, the user/individual on the job must be able to:

PC30: Hands-on design projects VLSI concepts.
PC31: Case studies of real-world applications
PC32: Presentation and discussion of project outcomes

2. Knowledge and Understanding (KU):

The individual on the job needs to know and understand:

KU1.Job candidates must have a strong foundation in Digital logic design fundamentals.

KU2. Candidates must have knowledge on Semiconductor Basics: MOS Physics, CMOS Technology,

KU3. In-depth knowledge of HDL – Verilog coding (Module and Testbench), Simulation, synthesis, Implementation, Extract the report and Analyze

KU4. Should have knowledge about Elements of RTL design and Strong debugging capabilities to identify and resolve issues.

KU5. Candidate should know ASIC design flow and should know about Design methodologies.

KU6. . Candidates should understand the CDC, CTS, logic synthesis process and its significance in digital design.

KU7. Candidates must develop skills in implementing STA, DFT, UVM features effectively in digital designs.

KU8. Should have knowledge about the principles of formal and advanced verification and its application in VLSI design.

KU9. Candidates must develop skills in using front-end design tools and methodologies, understanding the complete front-end design flow from specification to verification.

KU10. Should have knowledge about the various steps in the fabrication process, the challenges, and considerations in IC fabrication.

KU11. Candidates must have strategies in effective floor planning, placement, and Routing.

KU12. Candidates should develop skills in performing physical design verification and resolving violations.

KU13. Should have knowledge about DRC, LVS and ERC

KU14. Clear and comprehensive documentation of code, designs, and project-related information is essential for team collaboration and future reference.

3. Generic Skills (GS):

User/individual on the job needs to know how to:

GS1. Follow instructions, guidelines, and procedures.
GS2. Listen effectively and communicate information accurately.
GS3. Achieving the desired results.
GS4. Ethical usages of Development Board.
GS5. Logical Thinking & Analytical Skills

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Annexure: Assessment Criteria

Detailed PC-wise assessment criteria and assessment marks for the NOS are as follows:

Assessment will be carried out online , through the platform or offline in person , or in a blended format

PC No.	Assessment Criteria for Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
	Core: Fundamentals of VLSI Design & Semiconductors -15 hours *Mapped to* **: HCLT/N0046/IT/2024**	**5**	**0**	**-**	**-**
PC1	PC1. Introduction of MOS Device Physics, CMOS technology, VLSI Life cycle.	2	0	**-**	**-**
PC2	PC2. Apply the required logic to provide a solution for the problems	3	0	**-**	**-**
	Core: Getting Started with Digital Design & VLSI Representation – 15 hours *Mapped to* **: HCLT/N0046/IT/2024**	**5**	**10**	**-**	**-**
PC3	Introduction to Digital design	2	2	**-**	**-**
PC4	Combinational ,Sequential logic design and State machines	3	8	**-**	**-**
	Core: Essentials of RTL Verilog Coding -30 *Mapped to* **: HCLT/N0046/IT/2024**	**8**	**30**	**-**	**-**
PC5	PC5. Introduction to Hardware Description Languages	1	5	**-**	**-**
PC6	PC6. Basics of RTL Design - Verilog	1	5	**-**	**-**
PC7	PC7. Datapath building blocks- Combinational Elements and Sequential Elements of RTL Design	1	5	**-**	**-**
PC8:	Controller building blocks -State Machines	2	5		
PC9:	Memories	2	5		

PC No.	Assessment Criteria for Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
PC10	: RTL Methodology and Timing	1	5		
	Core: Getting Started with VLSI Design Flow Methodologies - 30 *Mapped to* **: HCLT/N0046/IT/2024**	**6**	**10**	**-**	**-**
PC11:	Steps in the physical design flow (RTL to GDSII) / ASIC design flow	2	-	**-**	**-**
PC12:	Design methodologies: Full custom, semi custom, Standard cell/ FPGA	2	10	**-**	**-**
PC13:	Design for manufacturability(DFM)	2	-	**-**	**-**
	Getting Started with Logic Synthesis & Optimization Process – 15 hours *Mapped to* **: HCLT/N0046/IT/2024**	**6**	**10**	**-**	**-**
PC14:	PC14: Objective of Logic Synthesis and Synthesis Flow	1	-	**-**	**-**
PC15:	PC15: Function for Synthesis and Constraints on Synthesis	2	4		
PC16:	PC16: 2-level and multi-level optimization	2	3	**-**	**-**
PC17:	PC17: Algebraic Model and Algebraic Model	1	3	**-**	**-**
	Fundamentals of Low Power Design Techniques – 15 hours *Mapped to* **: HCLT/N0046/IT/2024**	**6**	**10**	**-**	**-**

PC No.	Assessment Criteria for Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
PC18:	PC18: Sources of power dissipation: Dynamic and static power	2	-	-	-
PC19:	PC19: Power estimation techniques, Power optimization strategies	3	5	-	-
PC20:	PC20: Power Analysis (IR Drop)	1	5	-	-
	Essentials of VLSI Physical Design– 30 Hours *Mapped to* **: HCLT/N0046/IT/2024**	**8**	**20**	**-**	**-**
PC21	Overview of the physical design flow, Comparison between frontend and backend	2	-	-	-
PC22:	Circuit and Layout and IC fabrication	2	5	-	-
PC23:	Floor Planning, Placement and Routing	4	15		
	Essentials of VLSI Testing & Verification Methodologies -30 Hours *Mapped to* **:**	**6**	**10**		**-**
PC24:	Functional verification techniques and Formal verification methods	1	2		-
PC25:	Design for testability (DFT) and Testing methodologies and fault models.- Front end	1	1		
PC26:	Unified Verification Methodology (UVM)- Front end	1	2		
PC27:	Clock tree synthesis (CTS)	1	1		-
PC28:	DRC, LVS and ERC- Backend	1	2		
PC29:	Static Timing Analysis(STA)	1	2		
	Industry aligned projects – 30 hours *Mapped to* **: HCLT/N0046/IT/2024**				

PC No.	Assessment Criteria for Outcomes	Theory Marks	Practical Marks	Project Marks	Viva Marks
PC30:	Hands-on design projects VLSI concepts.	-	-	20	
PC31:	Case studies of real-world applications	-	-	20	
PC32:	Presentation and discussion of project outcomes	-	-	10	
	Total Score	**100**	**200**	**100**	
	Weightage	**50%**	**50%**	**50%**	
	Final Score	**50**	**100**	**50**	

Annexure: Assessment Strategy

This section includes the processes involved in identifying, gathering, and interpreting information to evaluate the Candidate on the required competencies of the program.

1. **Assessment System Overview and 2. Test Environment**

#	Functions	Feature (Career Shaper™)	Career Shaper™ Feature Description
1	**Test administration**	**Inbuilt Configuration manager**	**Examinee invitation, registration and slot scheduling with test monitoring controls**
1a	User management	Inbuilt user management	User creation and assigning to user groups
1b	Assessment Management	Inbuilt assessment management	Assessment scheduling, setup and controls
1c	Realm management	Inbilt Realm management	Institution (re-seller) creation and management
1d	Batch management	Inbuilt batch management	Slot creation and management with examinee assignment

2	**Test launch**	**Inbuilt test launch**	**Online web-based test launch with secure window feature**
3	**Testing & proctoring**	**Inbuilt test taking and proctoring**	**Supports major test types and formats, Image and screen proctoring**
4	**Scoring**	**Inbuilt scoring**	**Customizable scoring system**
5	**Instant reporting**	**Inbuilt reports**	**Customizable test reports available instantly for end-users**
6	**Data warehouse reports**	**Inbuilt data warehouse reports**	**Reports Factory built on PowerBI**
7	**Certificate generation**	**Inbuilt certificates**	**Customizable certificate templates**
#	**Functions**	**Feature (Career Shaper™)**	**Career Shaper™ Feature Description**
8	**Examinee Experience**	**Inbuilt EXP***	**Seamless examinee experience and clean UX/UI**
8a	Examinee Registration/ Profile updates	Inbuilt registration	Link based examinee registration, profile updation
8b	Examinee Test calendar & reschedule	Inbuilt Test calendar	Test and batch rescheduling
8c	Examinee onboarding & online assistant	Inbuilt examinee onboarding, AI based assistant (jordy)	Onboarding video and examinee user manual, Plugin available for online assistant
8d	Score Viewer & Download	Inbuilt result publishing	Instant Test score and report publishing to examinee
8e	Certificate Viewer & Download	Inbuilt certificate viewer and Download	Certificate publishing to examinee
8f	Skills & Job recommendation	Inbuilt recommendation engine	Skill & Assessment recommendation
9	**Technical Helpdesk**	**End-user tech support**	**Plugin available for end-user online tech support**
10	**Assessment Development**	**Inbuilt assessment development**	**Assessment Item and pack development**
10a	Item Creation & attribution	Inbuilt item creation	Assessment item creation and bulk item upload, classification & tagging

10b	Pack Creation & mapping	Inbuilt assessment pack creation	Assessment pre-packaging and test mapping configurations
10c	Randomization	Inbuilt randomization	Assessment item randomization
10d	Assessment item statistics	Inbuilt assessment item statistics	Item level examinee attempt statistics

3. **Assessment Quality Assurance levels/Framework:**

Assessment Quality Assurance framework ensures that the end-to-end activities encompassing the assessment life cycle consistently meet the intended objectives and meet the stakeholder satisfaction.

3.1 – Assessment Content Assurance

- Assessments are crafted based on our Industry Expertise, in consultation with practitioners and Subject Matter Experts (SME)
- The assessment methodology is based on scientific and well-established approaches to assessment design, development and validation. This is further validated by external consultants, experts with assessment and domain-related expertise.
- Assessments are designed, piloted and outcomes analyzed to ensure Face Validity, Construct Validity and Criterion Validity
- Sample QC checks are done on contents, to ensure alignment to outcomes.

1.2 – Assessment Platform Assurance

- Independent Testing of the platform functionalities is regularly conducted, using standard test cases and when enhancements and product bug fixes are implemented.

1.3 – Assessment Process Assurance

- Quarterly independent audits are conducted to validate process adherence.
- Findings recorded for action and monitored for effectiveness

Note: - The content and platform dimensions are customizable.

4. **Types of evidence or evidence-gathering protocol:**

- Assessments are hosted and deployed digitally on our secure, tested platform which enables logging of all transactions and footprints of users and enables greater traceability and transparency.

5. **Method of verification or validation:**

- Through digital verification of identity, proctoring functionalities and logs of all transactions on the platform

6. **Method for assessment documentation, archiving, and access**

- All assessment reports are available in HCL Tech archives for agreed on duration.
- Digital logs for each activity of each role holder recorded and stored with privacy and confidentiality requirements taken care of.
- Individual and group reports generated for each assessment event.
- Feedback taken from multiple stakeholders after assessment completion.

Annexure: Acronym and Glossary

Acronym

Acronym	Description
AA	Assessment Agency
AB	Awarding Body
NCrF	National Credit Framework
NOS	National Occupational Standard(s)
NQR	National Qualification Register
NSQF	National Skills Qualifications Framework

Glossary

Term	Description
National Occupational Standards (NOS)	NOS define the measurable performance outcomes required from an individual engaged in a particular task. They list down what an individual performing that task should know and also do.
Qualification	A formal outcome of an assessment and validation process which is obtained when a competent body determines that an individual has achieved learning outcomes to given standards
Qualification File	A Qualification File is a template designed to capture necessary information of a Qualification from the perspective of NSQF compliance. The Qualification File will be normally submitted by the awarding body for the qualification.
Sector	A group of professional activities on the basis of their main economic function, product, service or technology.